IBM Field Engineering

Instruction-Maintenance

7631 File Control Attachment

for 1302 Disk Storage

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IBM®

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Preface

This Field Engineering Instruction-Maintenance Manual describes the IBM 7631 File Control Attachment operation for 1302 Disk Storage. The manual contains four parts:

1. "Introduction" shows the difference between 1301 and 1302 disk storage. The 7631-1302 operational characteristics are also presented.
2. "Functional Units" describes VFO, shift register, and timing controls counter concepts.
3. "Theory of Operation" presents the circuit sequences that occur when writing the format or data tracks. The read sequences and data separation timing are also included.
4. "Maintenance Information" contains the adjustment procedures for the VFO, data separation, and gap detector circuits.

This manual is written at EC Level 254476.

To understand the information presented in this manual, the reader must know the 7631 principles of operation presented in the *IBM Customer Engineering Instruction-Maintenance Manual, 7631 File Control,* Form 223-2766.

Theory of operation and maintenance information for 1302 Disk Storage are presented in the following manuals:

IBM Customer Engineering Instruction Manual, 1302 Disk Storage, Form 227-5863.

IBM Customer Engineering Maintenance Manual, 1302 Disk Storage, Form 227-5864.

Copies of this and other IBM publications can be obtained through IBM Branch Offices.
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List of Illustrations

All IBM Customer Engineers are thoroughly familiar with IBM safety procedures; however, here are some reminders of general safety practices:

1. Do not work alone on the machine when power is on.
2. Wear safety glasses.
3. Be sure a fire extinguisher of the CO_2 type recommended for electrical fires is located in the room.
4. Turn DC off to prevent shorting when replacing a fuse or removing and inspecting SMS cards.
5. Discharge capacitors before working on DC power supplies.
6. Remember that 208 volts is present in the machine with power off.

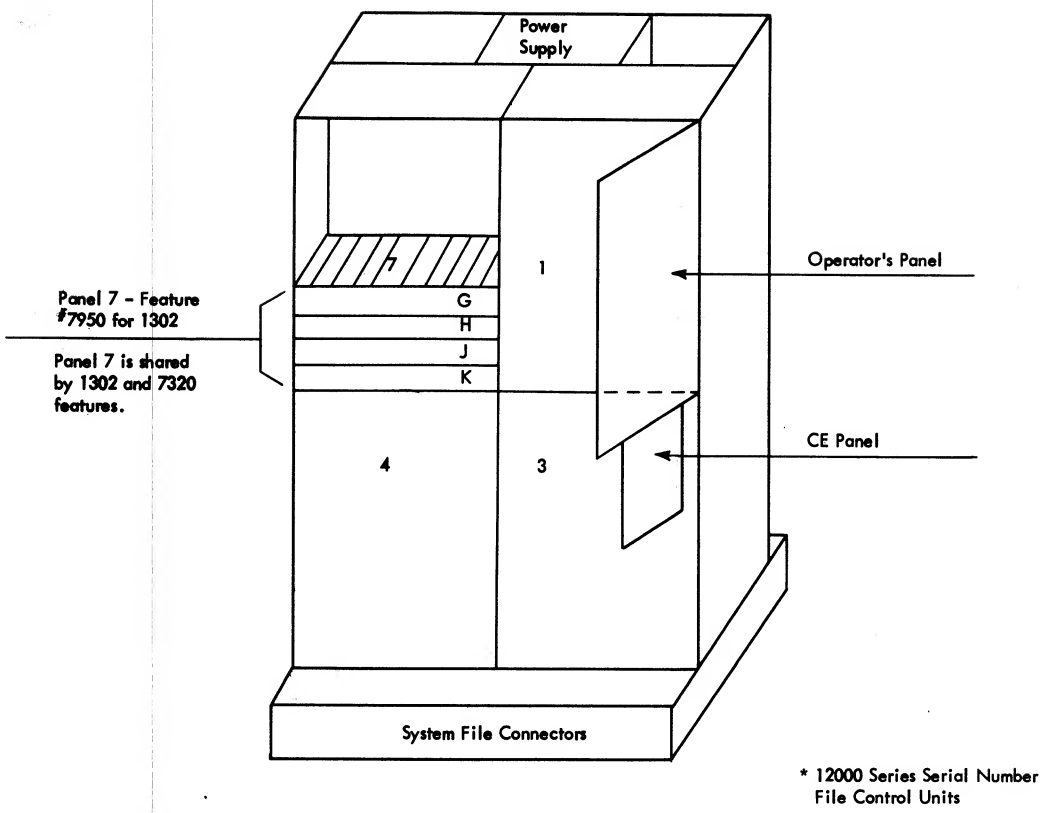


Figure 1. 7631 File Control with 1302 Attachment

Characteristic	1301	1302
Tracks per module	250	500
Track Capacity (6 bit characters one record per track)	2800	5850
Maximum character capacity per 2 module file (Model 2)	56 million	234 million
Maximum storage per 7631 (5 files - 10 modules)	280 million	1,170 million
Rotational speed average	1770 rpm	1770 rpm
Rotational delay average	17 ms	17 ms
Seek time maximum	180 ms	180 ms
Character average transfer rate	90 kc	184 kc

Figure 2. 1301-1302 Characteristics

7631-1302 File Control Attachment

- **7631-1302 File Control Attachment permits operation of 7631 File Control with 1302 Disk Storage.**
- **New write, erase, read, and timing concepts are used for 1302 operation.**

The 7631-1302 File Control attachment permits use of up to five 1302 Disk Storage Models 1 or 2, or up to five mixed 1301's, 1302's, and 7320's to a 12000 series serial number 7631 File Control. A 4 x 28 SMS card panel that is shared with the 7320 Drum Storage Adapter contains the 1302 attachment circuits (Figure 1).

The circuits modify the file control's write, erase, read, safety, shift register, and timing circuits for 1302 operation. File control operation with 1302 is different than its operation with 1301 because new write, erase, and read concepts are used for 1302 operation. The new concepts are used because the 1302's storage capacity and data transfer rate is greater than the 1301's. Figure 2 compares some of the 1301 and 1302 characteristics.

The following information presents the differences between the 1301 and 1302 operation and an understanding of the 7631-1301 operation is presumed.

1302 Disk Storage

- **Disks rotate at 1,790 rpm.**
- **New read-write heads are used.**
- **Tunnel erase permits 1302 disks to contain 500 tracks.**

Similar to the 1301, the 1302 magnetic disks are mounted on a vertical shaft. The shaft rotates, spinning the disks at 1,790 revolutions per minute. Because the 1302's bit density is greater than the 1301's, a new read-write head was designed to respond at a higher data frequency. The 1302 read-write heads fly closer to the disk surface than the 1301 read-write heads. A nominal read signal measured at the 1302 read-write head requires two to fifteen millivolts to go from an inner to an outer track.

Because the 1302 tracks are closer together than 1301 tracks, data written on a 1302 track spread close to the adjacent tracks. To prevent the flux from interfering with the adjacent tracks, the 1302 data heads have two erase gaps. These erase gaps are located behind the write gap; they erase or trim off the edges of the data tracks and confine the flux to a narrow band. This erase method, called tunnel erase, permits the 1302 disks to contain twice as many tracks as the 1301 disks.

Access Mechanisms

- **Two access mechanisms per module.**
- **500 cylinders per module.**
- **Each access mechanism spans 250 cylinders.**
- **Each access mechanism has 40 data, one format, and six alternate heads.**

Two access mechanisms per 1302 module span the 500 cylinders of 40 tracks each; each access mechanism spans 2½ inches, or 250 of the 500 cylinders. The two access mechanisms on the 1302 operate independently and may be in motion simultaneously. Each access mechanism is restricted to motion within its own zone of operation; access zero is used for the outer 250 cylinders and access one for the inner 250 cylinders. Figure 3 shows the location of each access.

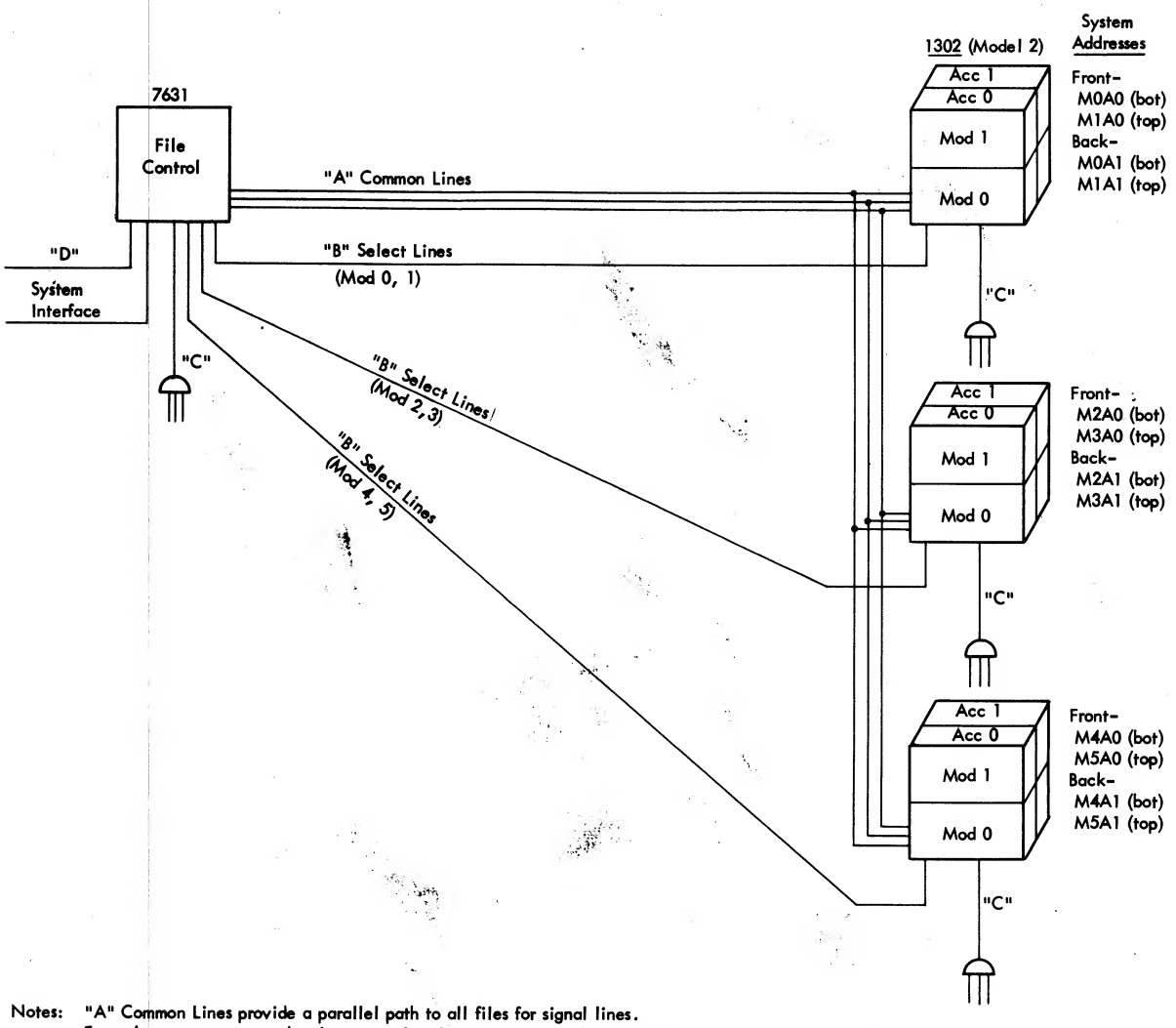
Each access mechanism has 40 data read-write heads, one format head, and six alternate surface heads. The access mechanism is hydraulically driven to simultaneously move all heads horizontally to any area of the 250 data cylinders of the access group.

Module Numbering

- **A module is a stack of 25 disks and two access mechanisms.**
- **A 1302 Model 2 contains two modules.**
- **Five 1302 Model 2's can be attached to one file control.**
- **Modules are addressed 0 through 9.**
- **The lower module is the even-numbered module.**

A stack of 25 magnetic disks (50 surfaces) with two associated access mechanisms make up a disk storage module. Of the 25 disks in a stack, 20 disks (40 surfaces) are used to store data. The remaining five disks (10 surfaces) are used for machine control and as alternate surfaces as follows:

Six surfaces are used as alternate surfaces. (The six alternate surfaces are used for flag tracks if a disk defect is encountered.)



Notes: "A" Common Lines provide a parallel path to all files for signal lines.
Examples: acc reg gates, head set, acc 0 or 1, write gate, and access ready.
"B" Select Lines gate a specific module for file operation.
Examples: module select and attention status.
"C" 1302 Power Cord, 208-230 volts, 3 phase, 60 cycle, 100 amp.
7631 Power Cord, 208-230 volts, 1 phase, 60 cycle, 30 amp.
"D" System Interface, 7000 Standard Interface or 1410-7010 Interface.

Select Line Assignments

7631 Cable Connection	1302 FF	and Module Address
01BU03	FF1	Mod 0,1
01BL05	FF2	Mod 2,3
01BU05	FF3	Mod 4,5
01BL07	FF4	Mod 6,7
01BU07	FF5	Mod 8,9

Figure 3. 1302 Addressing

One surface is used to provide format tracks.

Two surfaces (the top disk surface and bottom disk surface) are not used for data processing operations.

One surface is used for the clock track.

When five 1302 Model 2 units are attached to a 7631, a total of ten modules are available. Figure 3 shows module 0 is the lower module and module 1 is the top module. System addresses are shown on the right side of Figure 3. If five 1302 Model 2's are connected to one 7631, the system addresses are 0 through 9 for the ten modules; the even-numbered module is always the lower module.

Operational Characteristics

- **Control and sense (7000) operations are the same for 1301 and 1302.**
- **1302 access one attention status (7000) is included in the unused status bytes.**
- **Six-bit mode data is recorded at 184 kc.**
- **Eight-bit mode data is recorded at 144 kc.**
- **A clock bit is recorded with each data bit.**
- **The 7631-1302 clock circuits are independent of 1301 clock circuits.**
- **A 2.5-megacycle variable frequency oscillator (VFO) is the new timing source.**

All commands and orders, or instructions, defined for 7631-1301 operation are used identically for 1302 operation. Control and sense (7000) operations are the same for 1301 and 1302; the control and sense character transfer rates are also unchanged. Access one attention status information for 1302 is included in the last three bytes (not previously used) of the status word. Figure 4 shows the new status data bit assignments. Also, 1301 and 1302 seek times are the same. Because the rotational speeds of the 1301 and 1302 are the same, the average rotational delay to the given data area is the same.

The 1302 read, write, and write check operations differ from the 1301 in data transfer rates and the method of recording data. Data are recorded at 184-kc maximum rate in 6-bit mode and at 144-kc maximum rate in 8-bit mode. All 1302 data are recorded with clock bits to maintain high read reliability; that is, a clock bit is written prior to each data bit when writing on the data track (Figure 5). The 7631-1302 attachment contains the electronic circuits required to separate clock and data bits when reading. In addition, the 7631-1302 contains its own clocking circuits that are independent of those used for 1301 operation. A variable frequency oscillator (VFO) is the timing source for most 7631-1302 operations. The VFO operates at a nominal frequency of 2.5 megacycles or 400 nanoseconds per bit. Bit and digit ring operation are not changed, but the method of obtaining a selected phase is changed (Figure 6).

Format Track Write Clocking

- **The VFO is switched off and on with the gate VFO trigger.**
- **Clock track phase one is the selected phase when writing the index area.**
- **VFO timing is synchronized by phase one when writing system data.**
- **The VFO is designed to change frequency as the input sync changes frequency.**
- **The VFO holds its frequency in the absence of sync pulses.**

Two timing sources are used to write format. One timing source is the 640 kc clock track signal and the other source is the VFO output. The VFO is turned off and on with the gate VFO trigger (Figure 6). Figure 7 relates these timing circuits to the 7631 data flow diagram.

When writing the format index area, clock track phase one is gated as the selected phase to the delay line pulse generator. The delay line pulse generator outputs are used for write timing. Phase one is also used to write filler at the end of a format track (Figure 8, Line 1, Areas R and S).

The VFO signal is gated as the selected phase when writing system format write data and the required eleven filler characters. Figure 8 (Line 1, Areas A through Q) shows the areas written when the VFO is used for write timing. When the 7631 writes areas A through Q, clock track phase one is used as the VFO sync input; phase one keeps the VFO synchronized with the disk rotation speed.

Briefly, reliable VFO operation requires a sync input that does not vary more than a few nanoseconds from one bit to the next. For example, if phase one is used to sync the VFO, the VFO output is a continuous series of 2.5 megacycle pulses. If the disk speed decreases, the phase one frequency decreases. The VFO is designed to increase or decrease its output frequency as the phase one frequency changes with the disk speed. The VFO holds its sync frequency in the absence of sync pulses; if no sync pulses are applied for an extended period of time the VFO drifts back to its free-running frequency of 2.5 megacycles.

The clock track has an irregular spot that causes the VFO to malfunction. The irregular spot causes the clock track signal to vary when it is read. This variation pro-

hibits using the VFO for format index area writing; therefore, clock track phase one is used to write the index area filler.

Data Track Write Clocking

- **Format read data synchronizes the VFO when data writing.**
- **IBM 1302 on line inhibits the skew detector.**
- **The VFO free runs when filler is written.**

Data track writing uses the VFO two ways:

1. When data are written, the VFO is gated on and format read data is used to synchronize the VFO. Because format read data is not available in the format gaps that separate record and address areas, the last two data characters and the check characters are written while the VFO free runs. While the VFO free runs, it can hold its sync frequency to the end of check area.

2. The VFO is used for index area and filler bit writing without a sync input (Figure 6). Without a sync input the VFO oscillates at 2.5 megacycles (400 nanoseconds per cycle). Index area is written only when the order is an HAO-CE write operation.

Read Data Clocking

- **Raw read data is gated with the not block read data signal.**
- **Raw data must be separated.**
- **Raw data synchronizes the VFO.**
- **AFC clock bits correct the VFO frequency prior to setting the read gate.**
- **VFO outputs drive the separation circuits and the delay line pulse generator.**

Raw 1302 read data is gated into the 7631 with the not block read data signal. Raw read data flows to the data separation circuits and to the VFO circuits; raw data is used to gate and synchronize the VFO operation (Figure 6). Reliable reading needs precise timing to separate clock and data bits, to sample data at the output of data trigger A, and to drive the bit ring; therefore, all write data areas are recorded in two parts to permit reliable reading. The first part of each area contains automatic frequency control bits (AFC) and the second part contains the read data. The AFC contains seven characters of clock bits that are used to correct the VFO frequency before the read gate is set. (Details of the data areas are presented in the section, "Data Tracks.")

The read gate is set after the AFC bits correct the VFO frequency. The read data path from the data separation circuits to data trigger A is completed with the read gate (Figure 6). Clock and data bits are separated by the read data separation circuits.

VFO timing is used to operate the separation circuits and to drive the delay line pulse generator. The delay line pulse generator outputs are used to sample data at the output of data trigger A and to drive the bit ring. Bit ring timing gates the read data from data trigger B to the serial register, where characters are assembled.

Data control circuits are provided to prevent distorted clock pulses or stray bits from pulsing the VFO sync input. Without this protection a spurious bit might change the VFO frequency and cause a read error.

Data control circuit protection occurs at each end of a read data area. At the beginning of each address and record area the data control circuit activates the block read data signal for the first 16 microseconds of each address and record area (Figure 9). This blocks the first 15 AFC clock bits (approximately) from entering the VFO sync input. Because the write head current rises slowly, the first few AFC clock bits may be distorted; therefore, they are blocked. Data control circuit protection also occurs immediately after the last check character bit is read. The block read data signal blocks any AFC clock bits from the end of the last check character to the next address or record. If the next address or record is to be read, the data control circuit again blocks approximately the first 15 AFC clock bits.

Format Tracks

- **Format track area constants are different from 1301 area constants.**
- **Format writing must not exceed 640 kc.**
- **The VFO is used to write format system data and the required eleven filler characters.**
- **When the VFO is used to write, bits 0, 2, 4, 6, and 7 are not written.**
- **Bit 7 is always written prior to a gap.**
- **Phase one is used to write the index area.**
- **Simultaneous write and erase gate resets, at early index, create an unerased index filler area for head alignment.**

The format write operation follows the same sequence of commands as 7631-1301 operation with some changes.

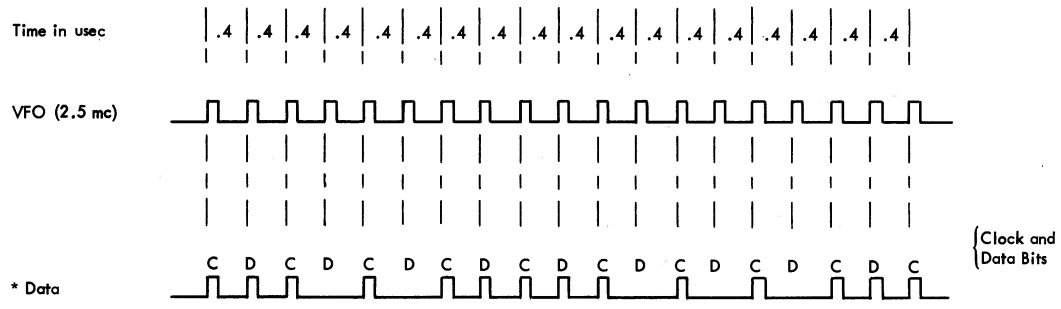
Format Data Area

Two basic changes in the format data area are:

1. The number of characters needed to define an address or record area.

Status Char	Bit No.	BCD Bit	Assignment	Comment
0	3	A	Reserved	
	5	4	Program Check	Summary
	6	2	Data Check	Byte
	7	1	Exceptional Condition	
1	3	A	Invalid Sequence	
	5	4	Invalid Code	Program
	6	2	Format Check	Check
	7	1	No Record Found	
2	3	A	Invalid Address	
	5	4	Response Check	Data Check
	6	2	Data Compare Check	
	7	1	Parity or Cyclic Code Check	
3	3	A	Access Inoperative	
	5	4	Access Not Ready	Exceptional
	6	2	File Frame Circuit Check	Condition
	7	1	File Adapter Circuit Check	
4	3	A	Channel Interrupt	
	5	4	Six Bit Mode	Optional
	6	2	Unassigned	Data Mode
	7	1	Unassigned	
5	3	A	Access 0, Module 0	
	5	4	Access 0, Module 1	Attention
	6	2	Access 0, Module 2	
	7	1	Access 0, Module 3	
6	3	A	Access 0, Module 4	
	5	4	Access 0, Module 5	Attention
	6	2	Access 0, Module 6	
	7	1	Access 0, Module 7	
7	3	A	Access 0, Module 8	
	5	4	Access 0, Module 9	Attention
	6	2	Access 1, Module 0	
	7	1	Access 1, Module 1	
8	3	A	Access 1, Module 2	
	5	4	Access 1, Module 3	Attention
	6	2	Access 1, Module 4	
	7	1	Access 1, Module 5	
9	3	A	Access 1, Module 6	
	5	4	Access 1, Module 7	Attention
	6	2	Access 1, Module 8	
	7	1	Access 1, Module 9	

Figure 4. Status Data Bit Assignment



** Bit Time	S	0	1	2	3	4	5	6	7	
BCD Value 1410		B1	WM	B	A	8	4	2	1	
BCD Value 7000		X	Q	B	A	8	4	2	1	Packed Alpha
BCD Value 7000		8	4	2	1	8	4	2	1	Packed Numeric

NOTES: * Character is a BCD A, in 8-bit Mode.
** 0.8 usec per bit.

Figure 5. Double Frequency Data

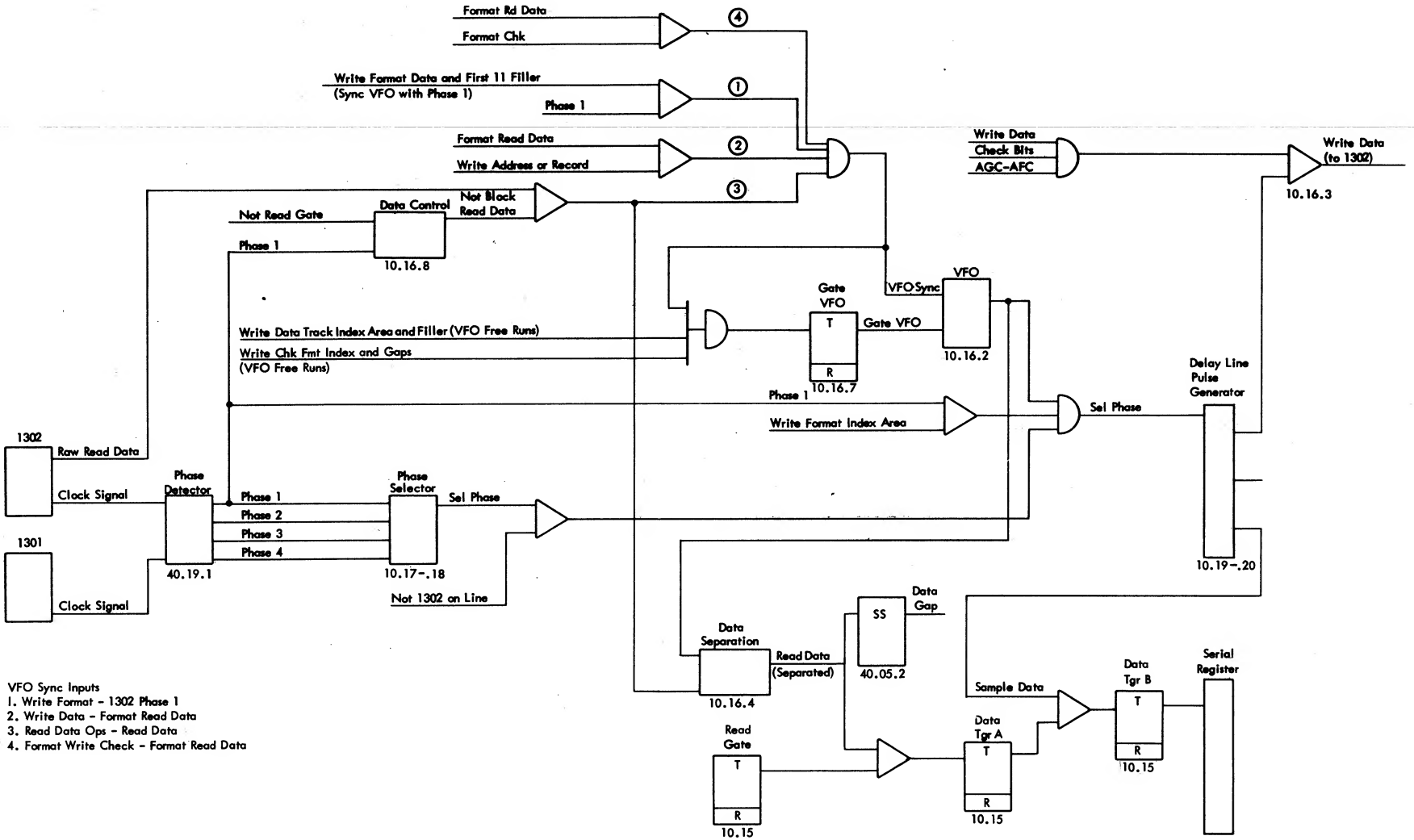
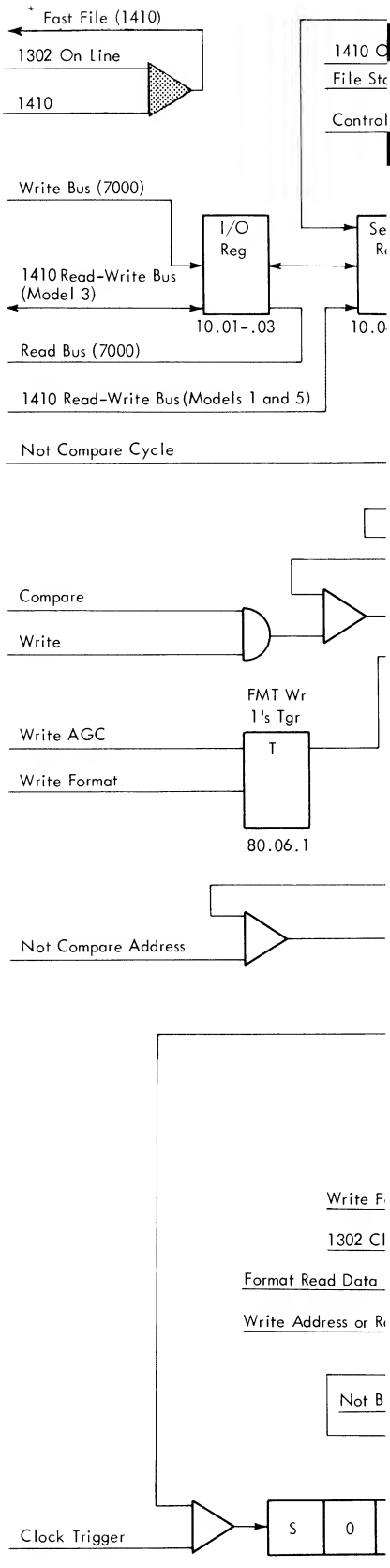
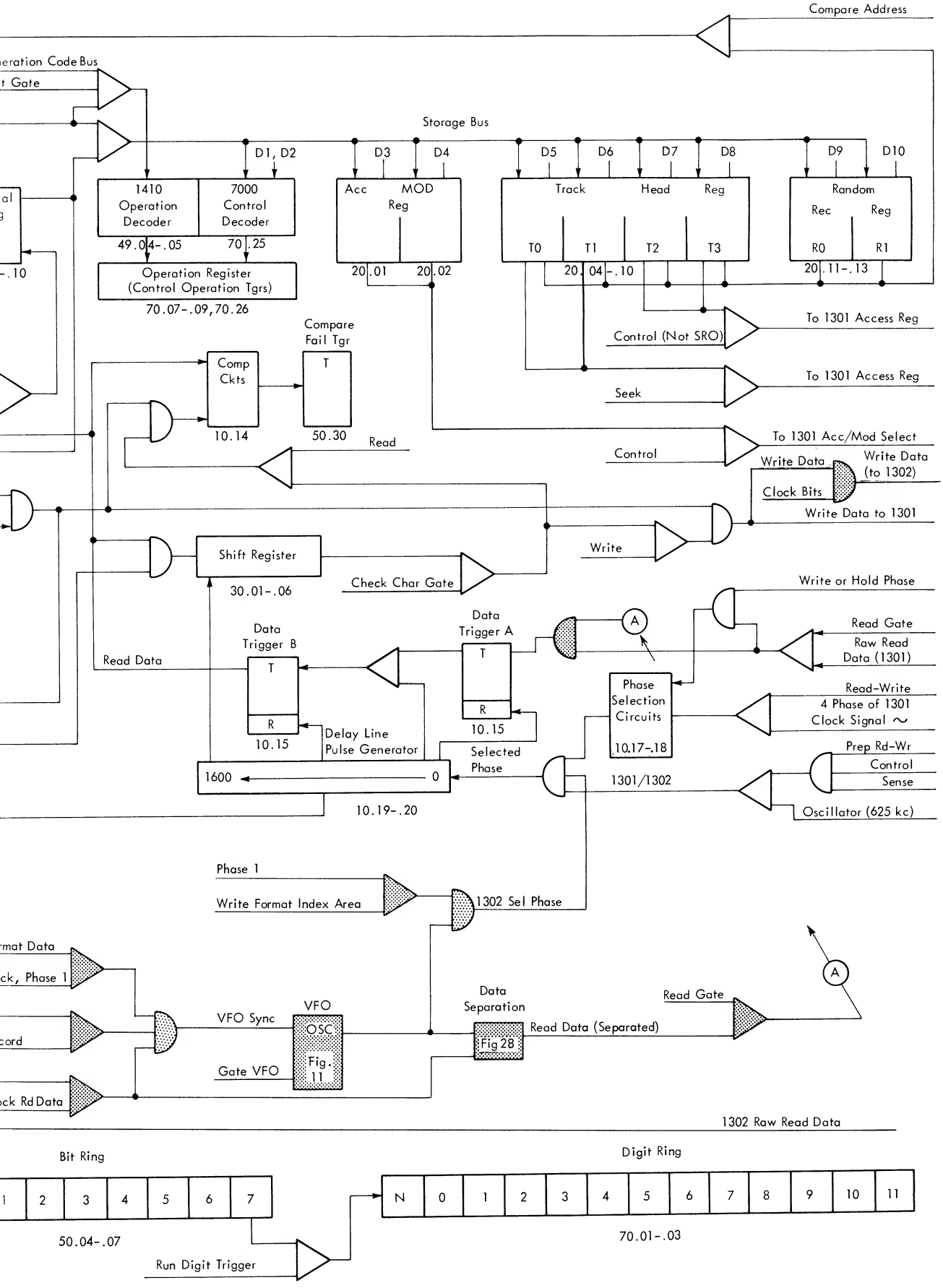


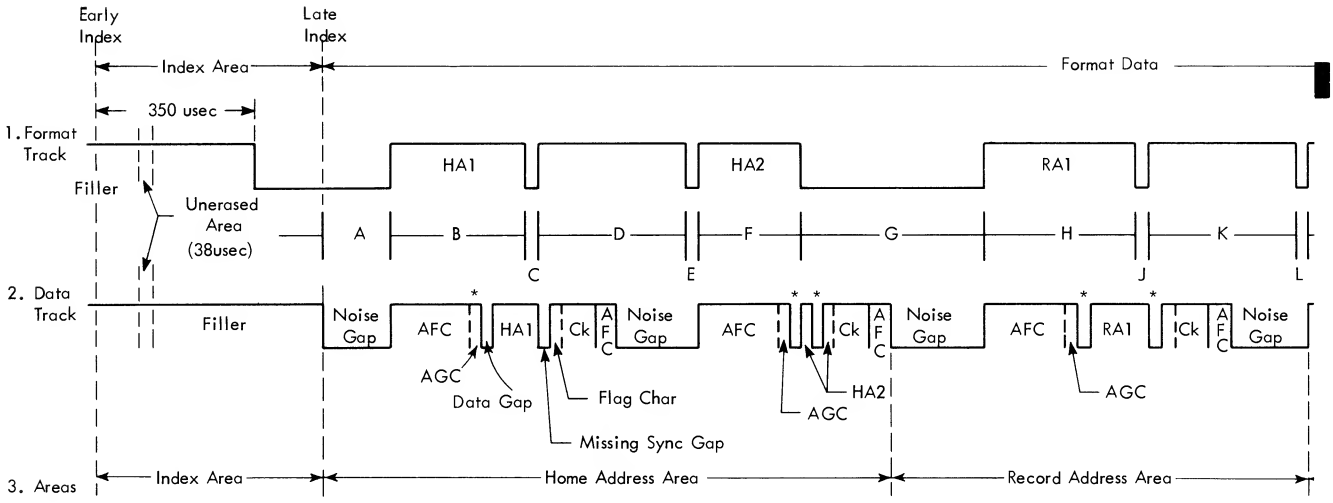
Figure 6. Simplified Timing Logic



*Fast File line inhibits 1410 overlap

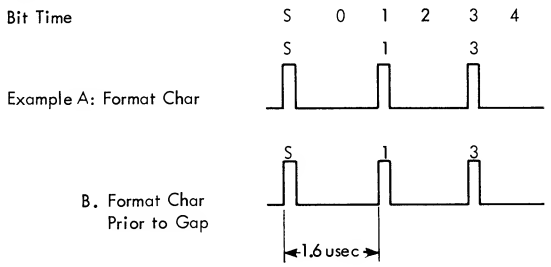
Figure 7. Data Flow Diagram


Compare Address
eration Code Bus
t Gate
Storage Bus
D1, D2
D3
D4
D5
D6
D7
D8
D9
D10
1410 Operation Decoder
7000 Control Decoder
49.04-.05
70.25
Operation Register (Control Operation Tgrs)
70.07-.09,70.26
Acc
MOD Reg
20.01
20.02
Track
Head
Reg
T0
T1
T2
T3
20.04-.10
Random Rec Reg
R0
R1
20.11-.13
Compare Fail Tgr
Comp Ckts
10.14
50.30
To 1301 Access Reg
Control (Not SRO)
Seek
Read
Control
To 1301 Acc/Mod Select
Write Data
Write Data (to 1302)
Clock Bits
Write Data to 1301
Write
Shift Register
30.01-.06
Check Char Gate
Write or Hold Phase
Data Trigger A
Data Trigger B
Read Data
Read Gate
Raw Read Data (1301)
Phase Selection Circuits
10.17-.18
Read-Write
4 Phase of 1301 Clock Signal
10.15
Delay Line Pulse Generator
Selected Phase
Prep Rd-Wr
Control
Sense
1600
0
10.19-.20
1301/1302
Oscillator (625 kc)
Phase 1
Write Format Index Area
1302 Sel Phase
rmat Data
ck, Phase 1
cord
ck Rd Data
VFO Sync
VFO OSC Fig. 11
Gate VFO
Data Separation
Fig 28
Read Data (Separated)
Read Gate
1302 Raw Read Data
Bit Ring
1 2 3 4 5 6 7
50.04-.07
Run Digit Trigger
Digit Ring
N 0 1 2 3 4 5 6 7 8 9 10 11
70.01-.03



* Data and missing sync gaps contain clock bits. Figure 10 shows area details.

Format Characters

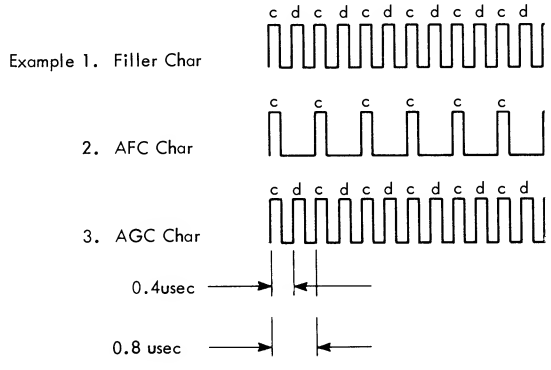


Format Area Constants

Area	Number of Characters	6 bit or 8 bit mode	BCD Code
A	6	8	4
B	12	8	3
C	1	8	4
D	13	8	3
E	1	8	4
F	9 minimum	6 or 8	1 or 3
G	15	6 or 8	2 or 4
H	13 minimum	6 or 8	1 or 3
J	1	6 or 8	2 or 4
K	13	6 or 8	1 or 3
L	1	6 or 8	2 or 4
M	9 minimum	6 or 8	1 or 3
N	15	6 or 8	2 or 4
P	1	6 or 8	2 or 4
Q	11 minimum	6 or 8	Controlled by 7631
R	0 minimum (see note 1)		
S	6 absolute	6 or 8	

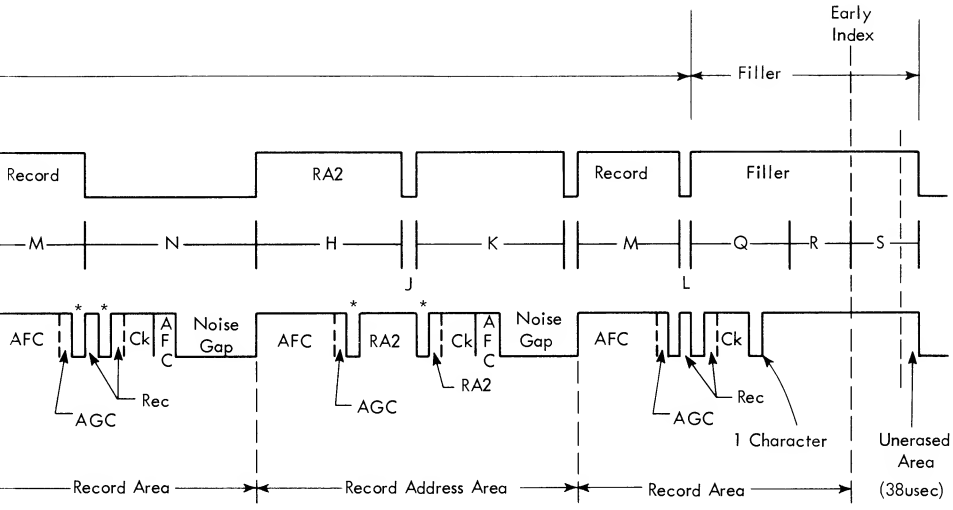
Areas F, H, and M must be 7 plus the desired number of data characters.

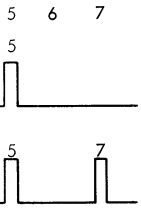
Data Track Characters

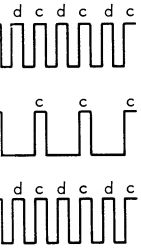


Note 1: Area R filler is needed when less than a full format track is written

Figure 8. Format and Data Tracks







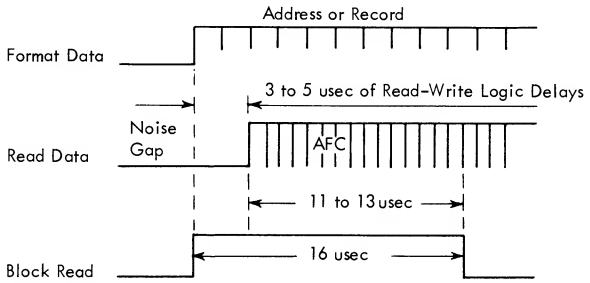


Figure 9. Block Read Timing

2. The number of characters in the gaps between addresses and records and between records and addresses.

First, the number of characters needed to define an address or record must be seven plus the number of characters desired in the corresponding data track area (Figure 8, Areas F, H, and M). The constant seven is needed to allow for the seven characters of AFC clock bits that are written at the beginning of each write data area.

Second, the gaps must be 15 characters long to allow for check characters and the space between the format head write and erase gaps. (Figure 8, Areas G, N, C+D+E, and J+K+L must each equal 15 characters.) Without the 15-character gap, the erase gap would erase some of the previous check characters when the write and erase gates are set for a write data area.

Format Data and Filler Characters

Another important change applies to writing format data and the first eleven filler characters. The 1302 format read amplifier cannot amplify a signal frequency that is above 640 kc; therefore, the 1302 format writing must not exceed 640 kc. Because the VFO is used for write timing when writing format data and the first eleven filler characters, a circuit is provided to reduce the 2.5-megacycle VFO writing frequency below 640 kc. Basically, the circuit prevents writing bits 0, 2, 4, and 6 with the not bit drive B signal. Eliminating the even bits does not quite halve the frequency; therefore, the circuit also prevents bit 7 from being written, except before a gap. Bit 7 of the last character before a gap is written to keep the gap singleshots from timing out too early. (See Figure 8, Format Character Examples A and B.) Because the remaining format track areas are written when clock track phase one is the timing source, the filler and index area bits are written at 640 kc.

Format Index Area

The final format change occurs in the index area; here, the write gate and erase gate are simultaneously reset at D6 of second index. Because the erase gap trails the write gap, 20 to 38 microseconds of the format index filler is not erased (Figure 8, Line 1). The unerased area is used to adjust the head to read from the center of the track.

Data Tracks

The 1302 data track contains six basic areas (Figure 8, Line 3):

- **Index Area**
- **Home Address One**
- **Home Address Two**
- **Record Address Areas**
- **Record Areas**
- **Filler**

Because the 1302 uses some new read and write concepts, the characteristics and organization of each recorded area are different from their 1301 counterparts.

Index Area

- **Clock and filler bits are written in the index area.**
- **Simultaneous write and erase gate resets at early index create an unerased index filler area for head alignment.**

The index area is defined with early and late index pulses. For most operations, late index signals the beginning of a data track, and early index signals the end of a data track. Clock and filler bits are written in the index area during an HAO-CE write. (Figure 8, Line 2 shows the index area filler, and Figure 8, Example 1 shows one expanded filler character.)

For HAO-CE write operations, the erase and write gates are reset simultaneously to create a 20 to 38 microsecond unerased area. The unerased filler is used to adjust the head to read from the center of the track.

Home Address One

- **The organization of HA1, HA2 record address and record areas, is changed.**
- **Changes that apply to HA1 also apply to the remaining data areas.**

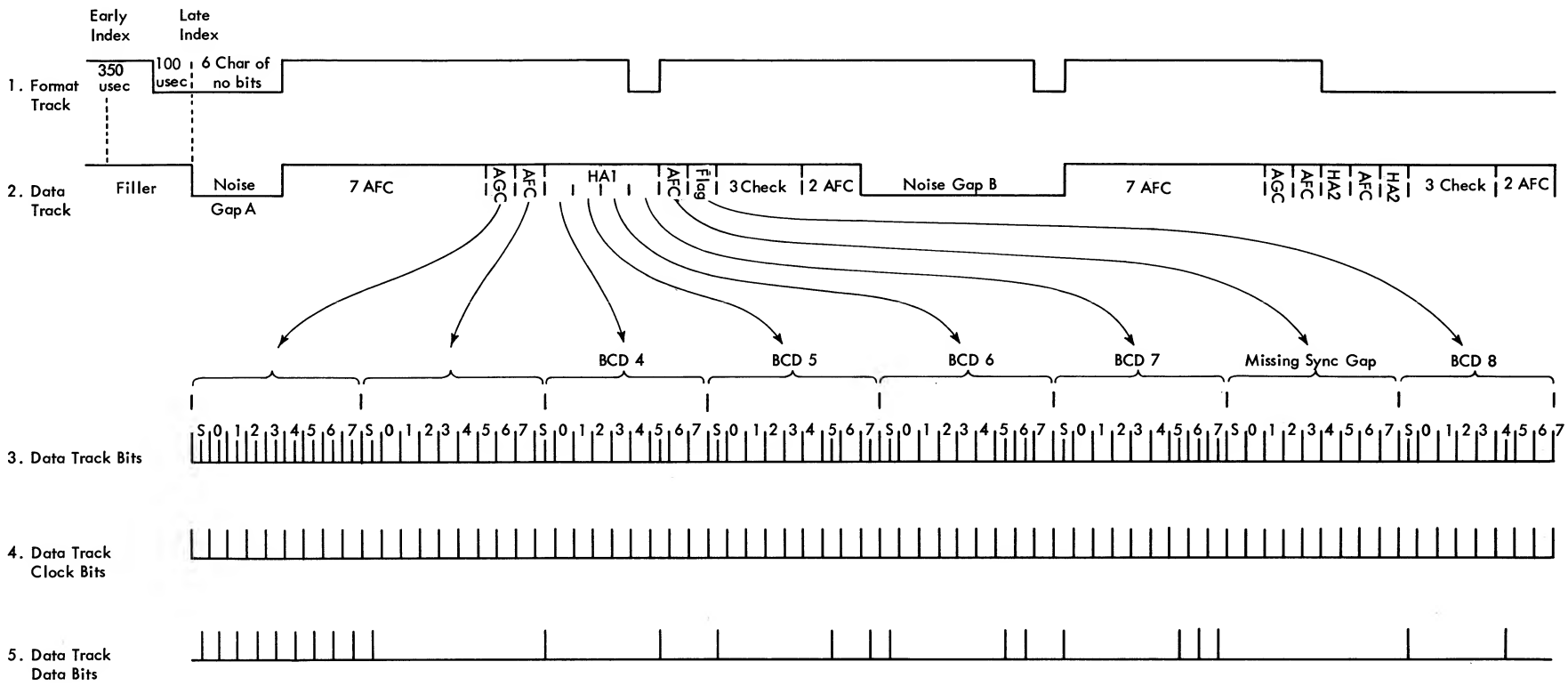
Home Address 1 (HA1) serves to identify the data track and to provide space for a flag character. Although the purpose of HA1 has not changed, its characteristics and organization have changed. Similarly, the purpose of HA2, record addresses, and records has not changed, but their characteristics and organization have changed. Figure 10 contains a list that shows the organizational changes to HA1.

The following text explains each part of HA1 and relates its purpose to file control functions. The changes to each part of HA1 also apply to the other data areas shown on Figure 8.

Noise Gap

- **A noise gap precedes each address and record area.**
- **Block read prevents the noise from entering the 7631 read data path.**

A six-character noise gap precedes the HA1 AFC (Figure 8, Line 2). The gap is created during an HAO-CE write



Name	Contents	* Number of Characters
Noise Gap A	A blank area	6
AFC	Clock bits	7
AGC	Clock and all 1-bits	1
AFC Data Gap	Clock bits plus sync	1
HA1	Clock and data to describe HA1	4
AFC Missing Sync Gap	Clock bits	1
HA1 Flag	Clock and flag data bits	1
Check Characters	Clock and check char bits	3
AFC	Clock bits plus sync	2
Noise Gap B	A blank area with noise	7

* All characters contain clock bits.
** Not used to sync the VFO.

Figure 10. Expanded Data Area

when the write gate is set and neither clock nor data are written. Because the 1302 data read amplifier operates at full gain and is not AGC biased, high amplitude noise appears at the read amplifier output when the gap is read. Figure 8 shows a similar noise gap precedes each address and record area. File control circuits are provided that block the noise and prevent it from entering the 7631 read data path. (See Figure 6, where block read data controls the read data flow into the 7631.)

Automatic Frequency Control (AFC)

- **Seven AFC characters are written in the first part of each address and record area.**
- **AFC clock bits are used to synchronize the VFO when reading.**
- **AFC clock bits are written every 800 nanoseconds.**

Seven characters of AFC clock bits are written in the first part of each write data area. The AFC clock bits are used to sync the VFO in subsequent read data operations. Because this area contains only clock bits, they are called single frequency recorded areas, or 1F areas. Figure 8, Example 2 shows one expanded AFC character. The character bit frequency is 1.25 megacycles or 800 nanoseconds per bit.

Automatic Gain Control (AGC)

- **One AGC character is written after the seven AFC characters.**
- **AGC contains clock and data bits.**
- **Separated data bits condition the data gap singleshot when reading.**

One AGC character is written adjacent to the last AFC character. The AGC character contains both clock and data bits. Because this area contains both clock and data bits, it is called a double frequency recorded area or a 2F area. Figure 8 (Line 2) shows where the AGC characters are recorded in each write data area, and Example 3 shows an expanded AGC character.

When reading, the data separation circuits separate the data from the clock bits; separated data bits appear on the Data A line to operate the 3-μs data gap singleshot (Figure 6). The separated data bits condition the 3-μs data gap singleshot; it times out in the following data gap and sets the read gate.

AFC Data Gap

- **The absence of data bits allows the data gap singleshot to time out when reading.**

One character of AFC clock bits defines the gap needed to separate AGC from the main body of HA1 (Figure 10). When this area is read, the absence of data bits on the Data A line allows the 3-μs data gap singleshot to time out; then the read gate is set (Figure 6). Figure 8 shows the location of the AFC data gap for each of the four basic data areas.

Home Address One (HA1)

- **Four characters of clock and data describe HA1.**
- **Clock and data are separated when reading.**

Four HA1 characters are recorded immediately after the AFC data gap; clock and data bits are recorded to describe HA1. Figure 10 (Line 2) shows the position of the main body of HA1. Figure 10 (Line 3) shows the bit sequence of clock and data that are recorded as HA1 for track 4567. Figure 10 (Lines 4 and 5) shows the HA1 clock and data bits as they would be separated by the read data separation circuit.

AFC Missing Sync Gap

- **One character of clock bits written to describe the gap.**
- **Missing sync bit identifies read mode check area.**

One character of AFC clock bits is written to create the missing sync gap. This gap is needed to define the read mode check area (Figure 10). When this gap is read, the sync circuits detect the missing sync bit; as a result, the sync bit missing signal is generated. Sync bit missing is then used to prepare the format recognition circuits to identify read mode check area.

HA1 Flag Character

- **The flag is written after the missing sync gap.**

The flag character is recorded after the missing sync gap. Figure 10 (Line 2) shows the position of the flag character. Figure 10 (Line 3) shows the clock and data that are recorded for HA1; the example shows the flag character is a BCD 8. To inhibit flag action, a BCD 8 or a blank is used; if the flag character is a BCD 1, 2, 4, 5, 6, or 7, flag action occurs. Notice that BCD 3 is not used.

Check Characters

- **Three characters of clock and data are written.**
- **IBM 1301 and 1302 check characters are the same.**
- **The shift register is modified to shift three times in 800 nanoseconds.**

Three check characters of clock and data are recorded after the last data character. Figure 8 (Line 2) shows their location on the data track. The check characters recorded for any given record are the same for 1302 as they would be for 1301; however, the shift register operation is modified for the 1302 feature. The shift register modification does not change the check char-

acters generated, but it does speed the shift register operation so it completes shifting in 800 nanoseconds.

Automatic Frequency Control (AFC)

- **Two characters of AFC clock bits complete check area.**

Two characters of AFC clock bits are recorded to complete the check area write mode operation. These two AFC characters are not needed but are written to complete the check area write mode timing. Figure 10 shows each character contains a sync bit.

The principal 7631 circuit changes required to make 1302 operation possible are timing changes. Phase selector A and B outputs are not used for 7631 read and write timing; instead, either clock track phase one or the VFO output is used for a selected phase. When clock track phase one is used for the selected phase, it is gated to the delay line pulse generator input. No other clock track phase is used for 1302 operation. When the VFO is used for the selected phase, it is necessary to know how it is controlled; because the VFO has four outputs, it is necessary to know their timing relationships.

VFO (Variable Frequency Oscillator) Operation

- **The VFO is a 2.5-megacycle oscillator.**
- **Gate VFO trigger gates the VFO off and on.**
- **The VFO can free run at 2.5 megacycles or correct to an input sync frequency.**

The VFO is basically a 2.5-megacycle oscillator that has two inputs and five outputs. One input, gate VFO, gates the VFO off or on; the other input, sync bits, is used to synchronize the VFO with the disk when reading or writing data. When gate VFO is on, the VFO oscillates at 2.5 megacycles; if sync pulses are applied to the VFO while the gate is on, the VFO corrects to the input sync pulse frequency.

Physically, the VFO is contained on two SMS cards. The ramp card contains an oscillator, a pulse generator, and a binary trigger; there are five outputs from this card (Figure 11, Pins T, U, X, W and B). When the gate VFO signal is off, the outputs are reset to the polarities shown on Figure 11 (Lines 3 through 6). The error detector card contains circuits that generate a correction current; the correction current controls the VFO frequency. Correction current flows from pin V of card 7J13 to pin C of 7J12. In addition, error detector card pin T output resets the ramp card when the gate VFO signal is off.

VFO operation starts from the reset state; while reset, the ramp output is clamped to zero volts (Figure 11, Line 3). When gate VFO is set, the ramp output increases to +3 volts; the oscillator feedback then causes the ramp output to fall to −3 volts. During the ramp's transition from +3 to −3 (about 35 nanoseconds) the pulse generator fires; it produces the 150 nanosecond 2F VFO pulse (Figure 11, Line 4). This pulse also flips the binary trigger. Figure 11 (Lines 5 and 6) shows the ramp card binary trigger outputs.

The gate generator output occurs when the VFO ramp input fires the gate generator (Figure 11, card 7J14). The ramp gate's rise and fall are adjustable. The rise and fall adjustments are made with respect to read data delayed (Figure 11, Line 8); therefore, the read data delay adjustment must be completed first. The read data delay adjustment is made to position the leading edge of a read data bit 160 nanoseconds prior to the next transition of the binary trigger. (Complete adjustment procedures are in the maintenance section of this manual). The ramp gate is adjusted to rise 140 nanoseconds prior to the leading edge of read data delayed (Figure 11, Lines 7 and 8). The ramp gate fall is adjusted to drop 250 nanoseconds prior to the leading edge of the next clock bit.

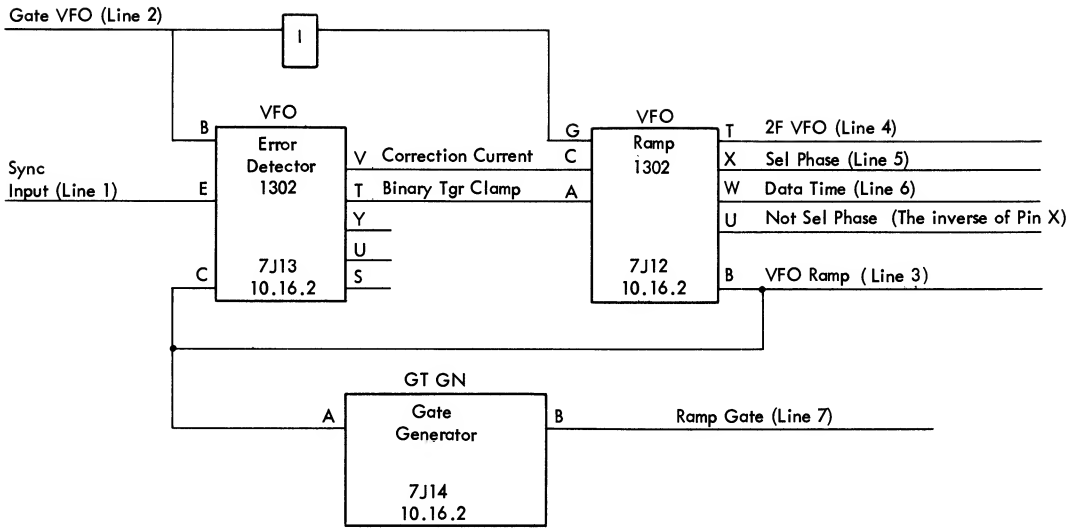
Depending on the type of 7631 operation, the VFO may be operated with or without sync bits. The example operation on Figure 11 shows the VFO is synchronized with read data. The error detector card compares the sync input (Pin E) with the VFO ramp input (Pin C) to determine the change in the correction current. When the sync input occurs at the ramp center, the correction current remains unchanged; if the sync input occurs before or after the ramp's center, the error detector generates correction current that changes the VFO frequency accordingly.

Shift Register

- **Shifts three times in 800 nanoseconds.**
- **Is tested prior to writing each address and record area.**
- **A test failure causes an FA circuit check.**

Because the 1302 bit cycle is only half as long as that of the 1301, the shift register has been modified to shift faster. The 16 shift register positions shift with three pulses during an 800-nanosecond interval. The 1302 shift register generates the same check characters as the 1301 shift register, but the triggers are shifted in a different sequence at a faster rate (Figure 12).

A shift register test is performed before writing each address or record area. Twenty-eight AGC data bits and two zero bits are entered for the test. The shift register resets are adjusted to allow the correct number of one



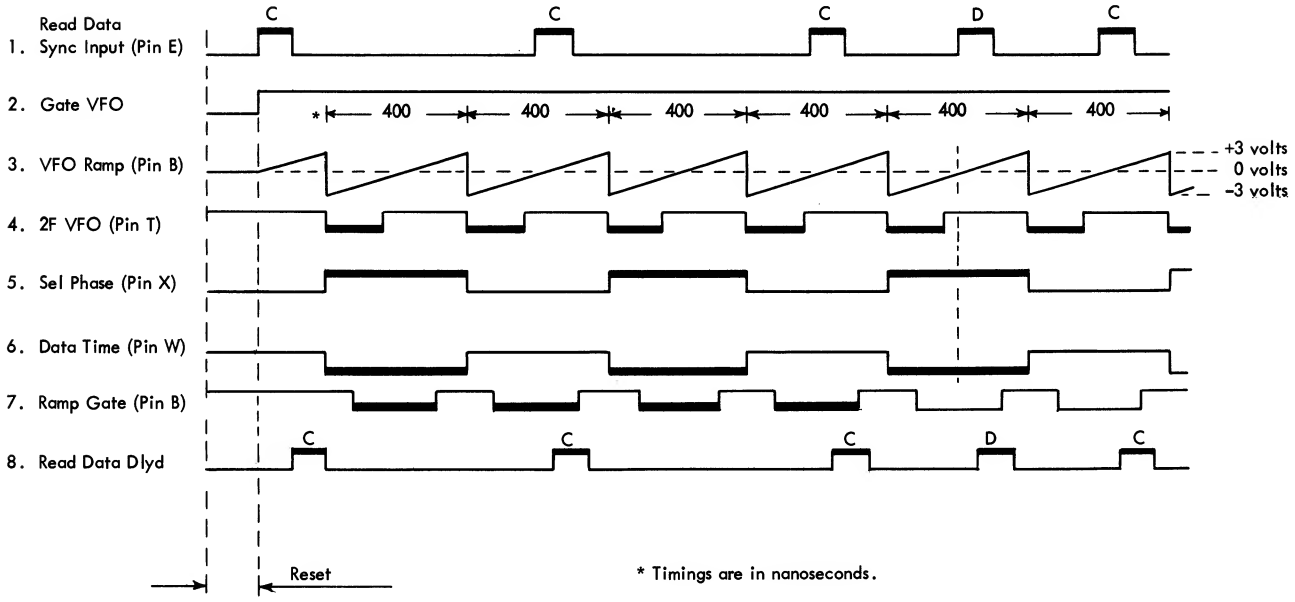


Figure 11. VFO Timing

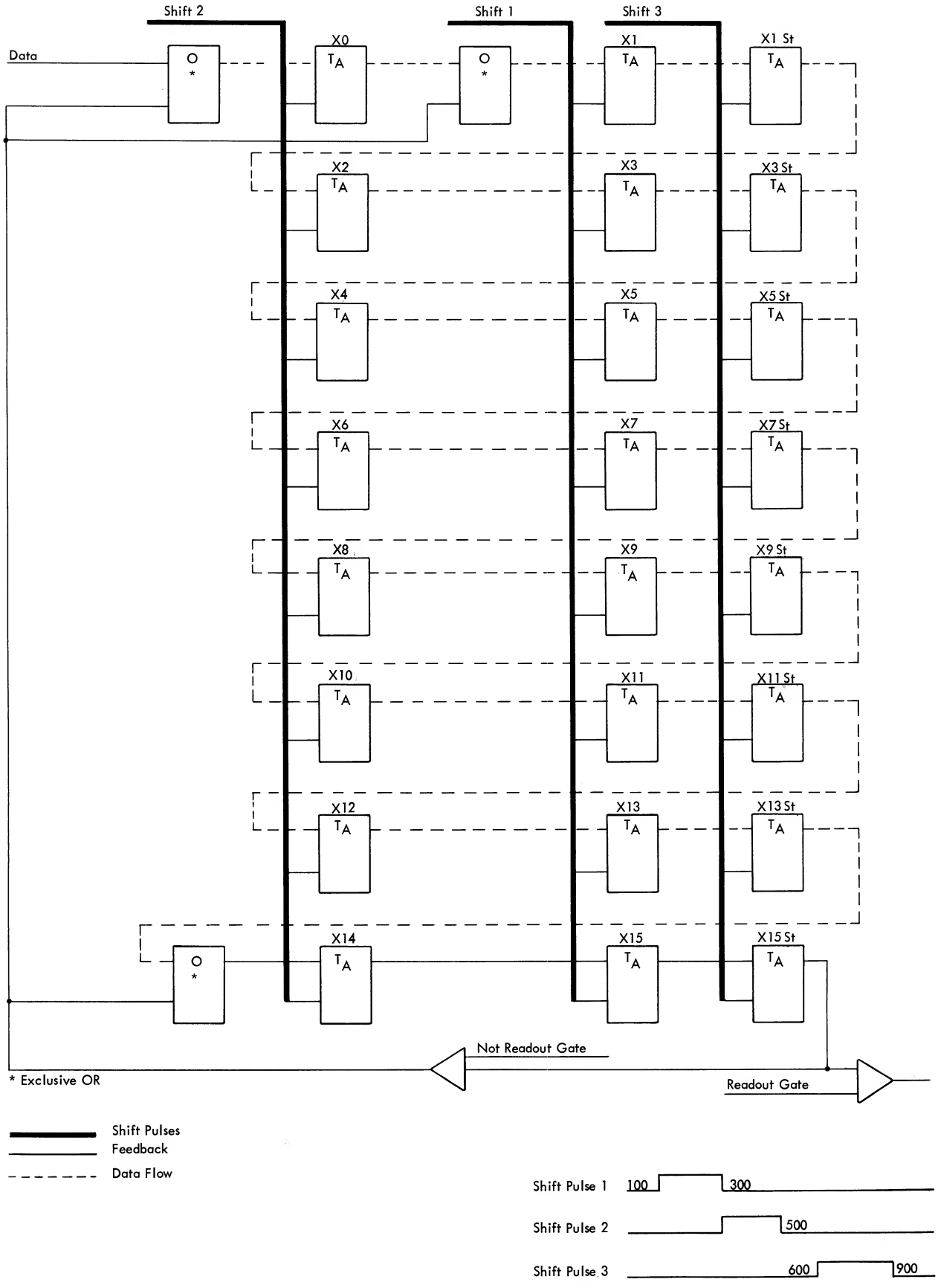


Figure 12. Shift Register

and zero bits to enter the register before the test for both bit modes of 1301 and 1302 operation (Figure 13).

Failure to enter the correct number of bits or any shift register failure is detected by a test. A test failure causes a file adapter circuit check (Figure 13). The shift register test timing is shown on Figure 33 in the Maintenance Information section of this manual.

Timing Controls Counter

- **Controls raw read data flow into the file control.**
- **Controls the erase gate reset except for HAO-CE and format write.**
- **Controls the safety circuits.**

The timing controls counter is used to:

1. Control raw read data gating in the 7631.
2. Reset the erase gate 38 microseconds after the write gate reset to insure all data are tunnel erased.
3. Control the safety circuits.

Counter Operation

Machine idle reset sets the count 16 and 32 triggers and resets the remaining counter triggers. Count 48 blocks the input count gate. Receipt of address, record, write gate, or not write gate resets the 48 count and starts a counter sequence. Counter operations end at machine idle reset or count 48 (Figure 14).

Erase Gate Reset for TWA or End Operations

When the write gate is reset for TWA record address areas or at the end of any write operation, except format or HAO-CE, a counter sequence starts. The counter sequence has four purposes.

First, count 24 is used to reset the erase gate. The 38-microsecond delay insures all data are tunnel erased. (Figure 15, Lines 5 and 6.)

Second, write 34 count trigger activates suppress safety check (Figure 14). The first 40 microseconds of suppress safety check blocks read safety and write monitor file frame circuit checks. Suppress safety check is needed because read safety rises before the write monitor is reset (Figure 15, Lines 7 and 8).

Third, simulate read safety is needed to block the read monitor and not read safety file frame circuit check. Simulate read safety is needed because the read monitor is set before read safety can return from the 1302 (Figure 15, Lines 4, 8, and 9). Notice that the simulate read safety trigger is set with count 2. The two-count delay is needed because simulate read safety has less logic delay to the safety circuits than suppress safety check. If simulate read safety is not delayed to allow time for suppress safety check to rise, read safety simulated and write monitor would cause a file frame circuit check (Figure 15, Lines 4, 7, and 8).

The previous three counter functions are used to end all 7631-1302 write operations except format and HAO-CE write. At count 24, 38 microseconds, machine idle reset completes most 7631 operations. If the write gate fall occurred when B1, D5, check area, and record holdover AND for TWA, machine idle does not occur and the full 34 count sequence is needed.

Fourth, the last ten counts of suppress safety check block the read monitor and write safety file frame circuit check. The last ten counts allow time for write safety to drop after the erase gate reset for TWA write operations (Figure 15, Line 9).

Set Write Gate

When the write gate is set, the timing controls counter starts a ten-count sequence (Figure 14). First, the write safety is simulated to block the write monitor and not write safety file frame circuit check because write safety rises slowly in the 1302 (Figure 15, Lines 11, 12, 13, and 16). Second, suppress safety check blocks write monitor and read safety file frame circuit check. Read safety is slow to fall because it is delayed by the slow erase gate rise in the 1302 (Figure 15, Lines 12, 14, and 15).

Block Read

The counter generates block read for all address and record areas. The ten-count block read signal blocks raw read data flow to the VFO and data separation circuits until count 10 falls. Block read causes the 7631 to skip the disk noise areas and the first few AFC clock bits to insure proper VFO operation. Figure 26 (Line 4) shows how block read applies to a read operation.

Because the record area signals are set with check area timing for read HAO-CE operations, the block read signal is needed for a longer period of time. Figure 14 shows the block read on HAO signal is up for 34 counts. Figure 26 (Line 14) shows the application of block read on HAO.

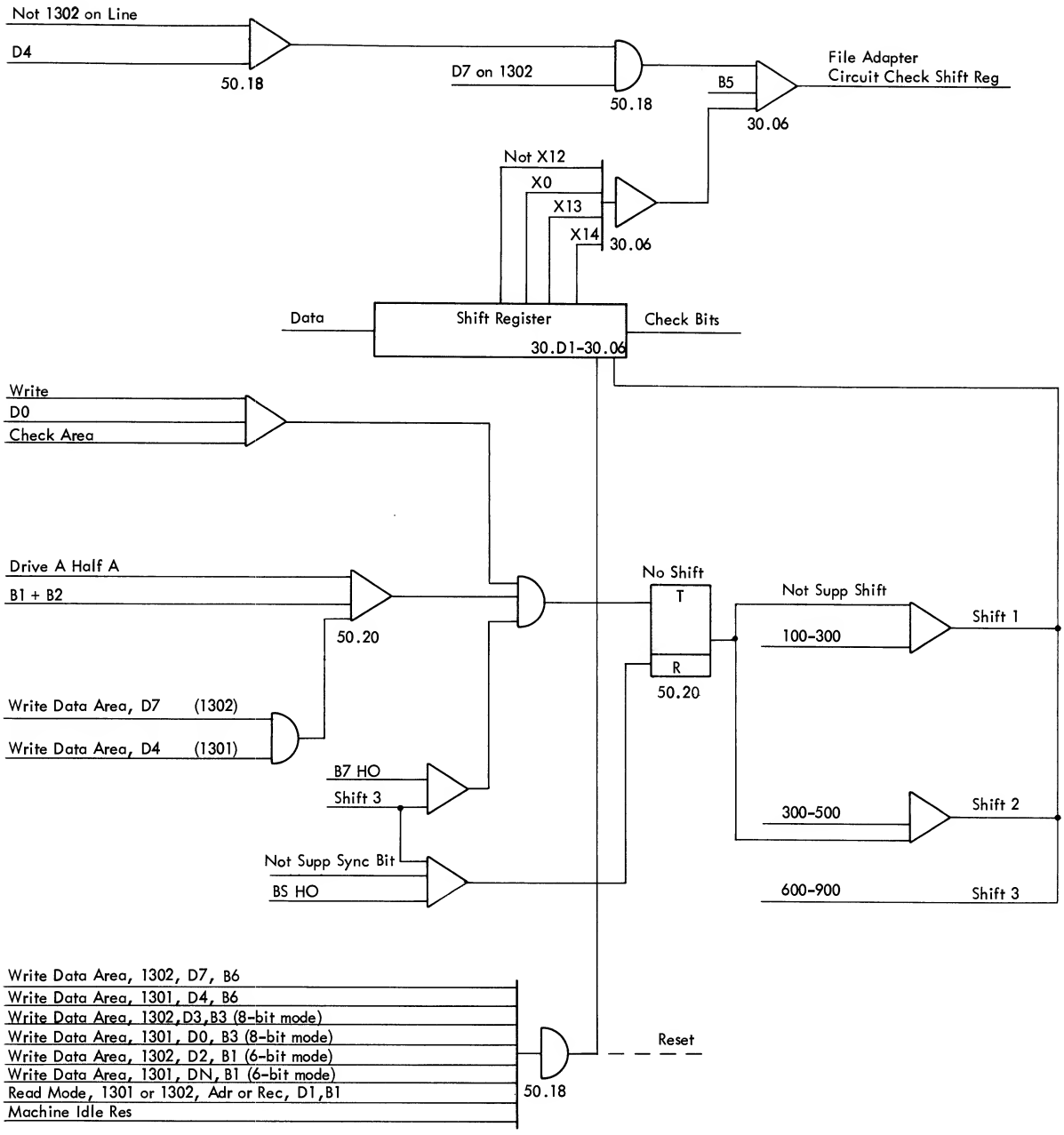


Figure 13. Shift Register Controls

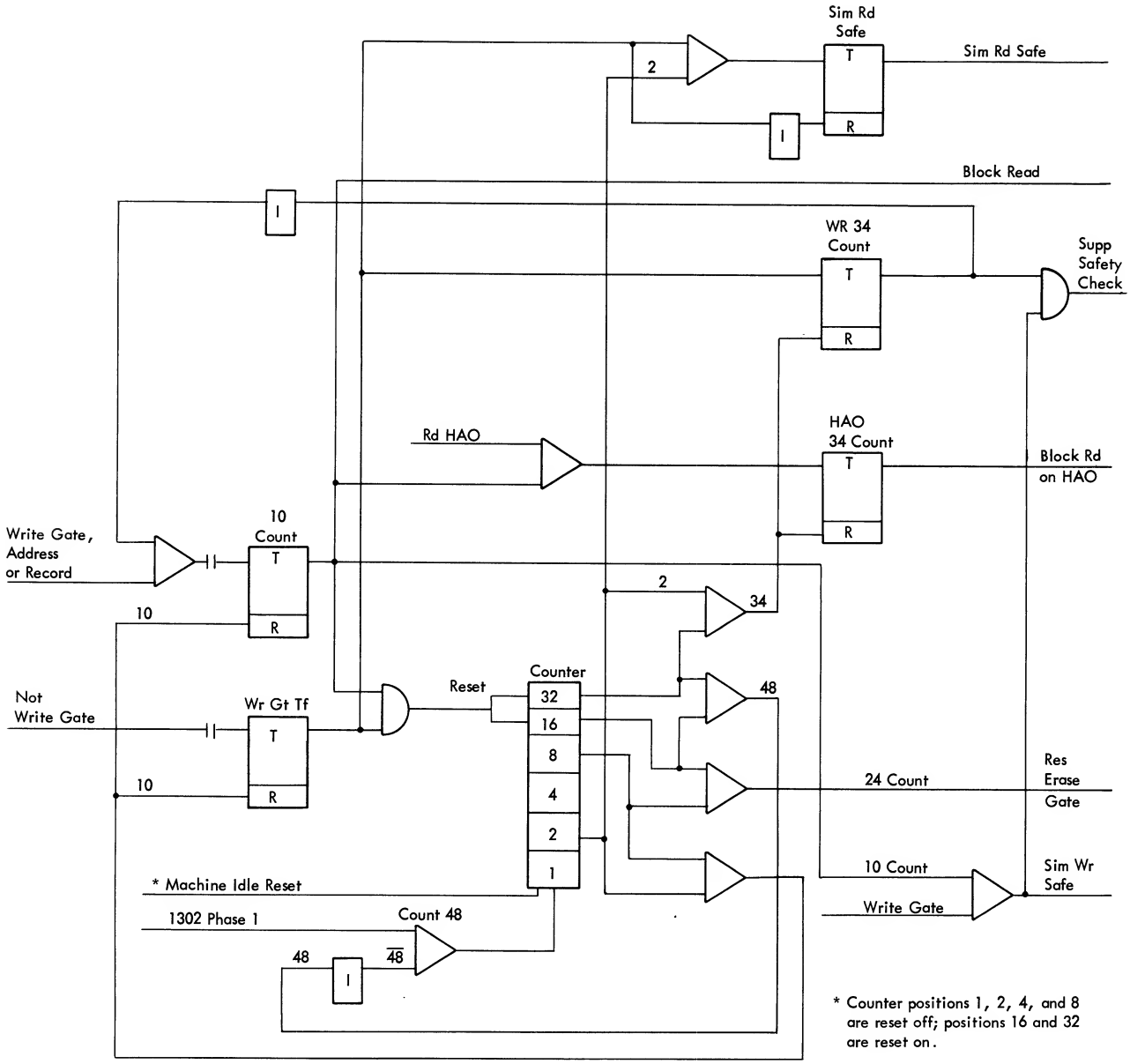


Figure 14. Timing Controls Counter (ALD 10.16.9)

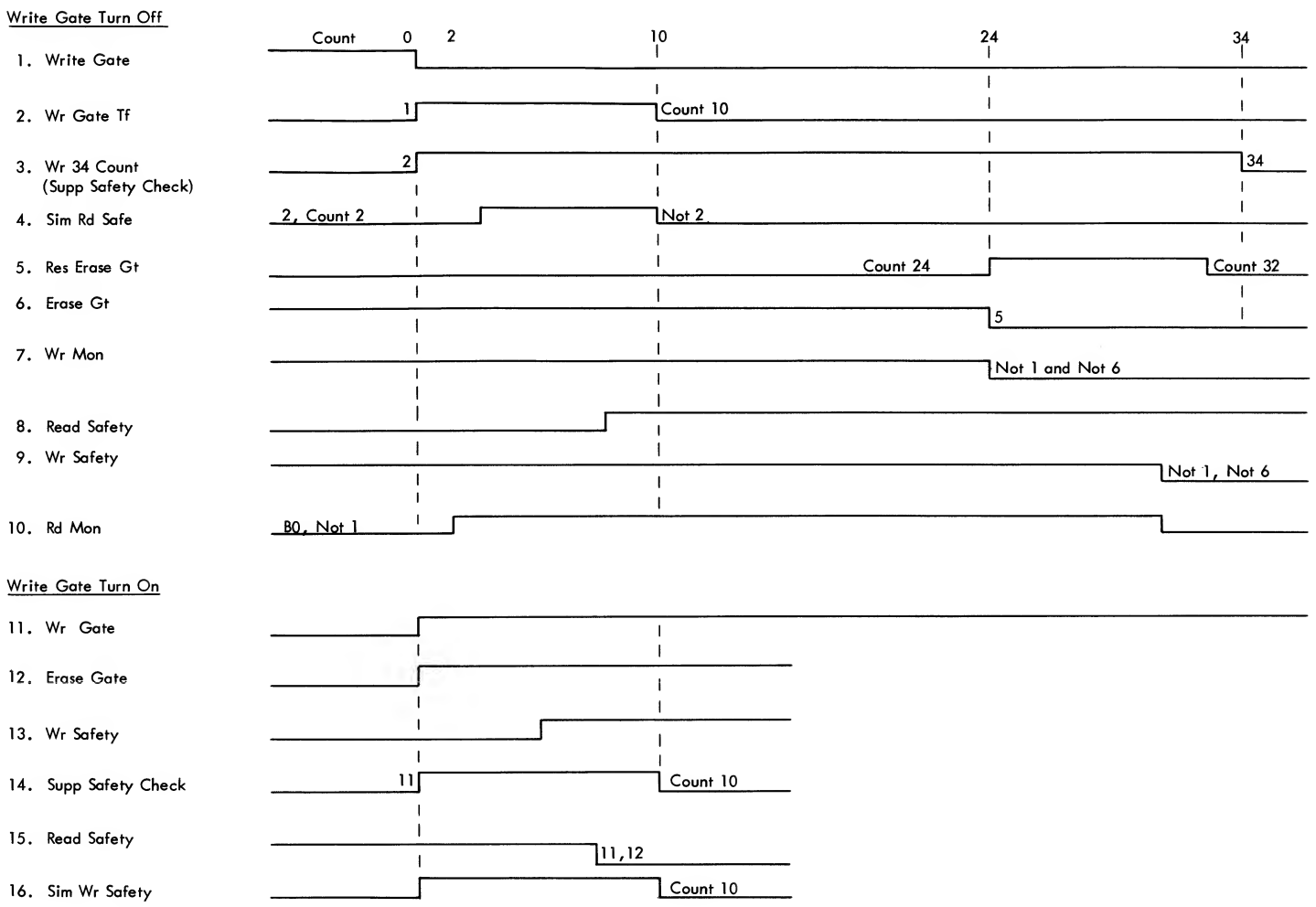


Figure 15. Timing Controls Counter Outputs

Format Write

- **Phase one is used to write the index area.**
- **VFO timing is used to write system data and the required eleven filler characters.**
- **The VFO is synchronized with phase one pulses.**

The format write operation for 1302 differs from 1301 format write only during the time the write gate is set. The write portion of the operation is divided into two parts:

1. Index area writing.
2. Format data writing.

Index area writing is needed to record 350 microseconds of index area filler bits. Clock track phase one is used for the selected phase input to the delay line pulse generator when writing the index area filler. When the 7631 writes data, the system write data (BCD 1, 2, 3, or 4) is decoded and all one-bit or all zero-bit characters are recorded to describe the 1302 format track. The VFO output is used for the selected phase input to the delay line pulse generator when writing system data. New timing and write circuits are used for 1302 operation. Figure 16 shows the timing circuits (Areas 12A and 13A) and the write circuits (Areas 12D and 13D).

Index Area

- **Bit ring timing is needed to set write gate and write monitor.**
- **AGC squelch singleshot causes index area filler writing.**

The objectives are to:

1. Gate the selected phase to the delay line pulse generator input.
2. Set the format write ones trigger and write 350 microseconds of filler bits.
3. Run the bit ring two cycles.
4. Set the write and erase gates.

Clock track phase one is gated to the delay line pulse generator input with format write and not record holdover (Figure 16, Area 12A). The delay line pulse generator outputs are available when prep read-write drops and select ACU rises; these signals gate the selected phase. The data AGC squelch condition sets the format write ones trigger; the format write ones trigger is the write data source that is used to set the write data latch when format writing. Figure 16 (Areas 9C and 10D) shows the AGC squelch and format write ones trigger.

Bit ring timing is needed to set the write gate and start the index area writing. The clock trigger is set with run clock on format or HACE (Figure 16, Area 5D) to start the bit ring; run clock on format or HACE is a result of the data AGC squelch signal gated with not write monitor. When the clock trigger is set, the bit timing sets the write gate; B1 sets the write gate, the write gate sets the erase gate, and the next B0 sets the write monitor. The write monitor trigger drops run clock on format or HACE; this allows the next BS to reset the clock trigger. The bit ring stops at the next BS; bit ring timing is not needed to continue the index area writing. Figure 17 shows the format write timing sequence needed to start the index area writing.

Index area write data flow from the AGC squelch singleshot to the write driver is shown on Figure 16 (Areas 9C through 13D). Figure 18 shows the timing details for index area writing. Index area writing stops when the data AGC squelch singleshot times out and causes the format write ones trigger to reset. The write gate remains set when filler writing stops to create the gap between index area filler and late index.

Data Area

- **Use VFO timing to write.**
- **Synchronize the VFO with phase one.**
- **Block writing bits 0, 2, 4, 6 and 7.**
- **Write bit seven prior to each gap.**

The objectives are to:

1. Start the VFO and use the pin X output for the selected phase.
2. Gate clock track phase one to synchronize the VFO.
3. Block phase one from the selected phase line.
4. Start the bit ring.
5. Write all ones or all zeros characters to describe the format track.

The key signal used to control format data writing is run clock on format write. When run clock on format write is active, the following sequence occurs:

1. Phase one pulses are gated to set the gate VFO trigger (Figure 16, Area 6A; Figure 17, Line 10).
2. Phase one pulses are gated to synchronize the VFO (Figure 16, Area 8A; Figure 17, Line 11).
3. Gate VFO starts the VFO (Figure 16, Area 9A; Figure 17, Line 10).

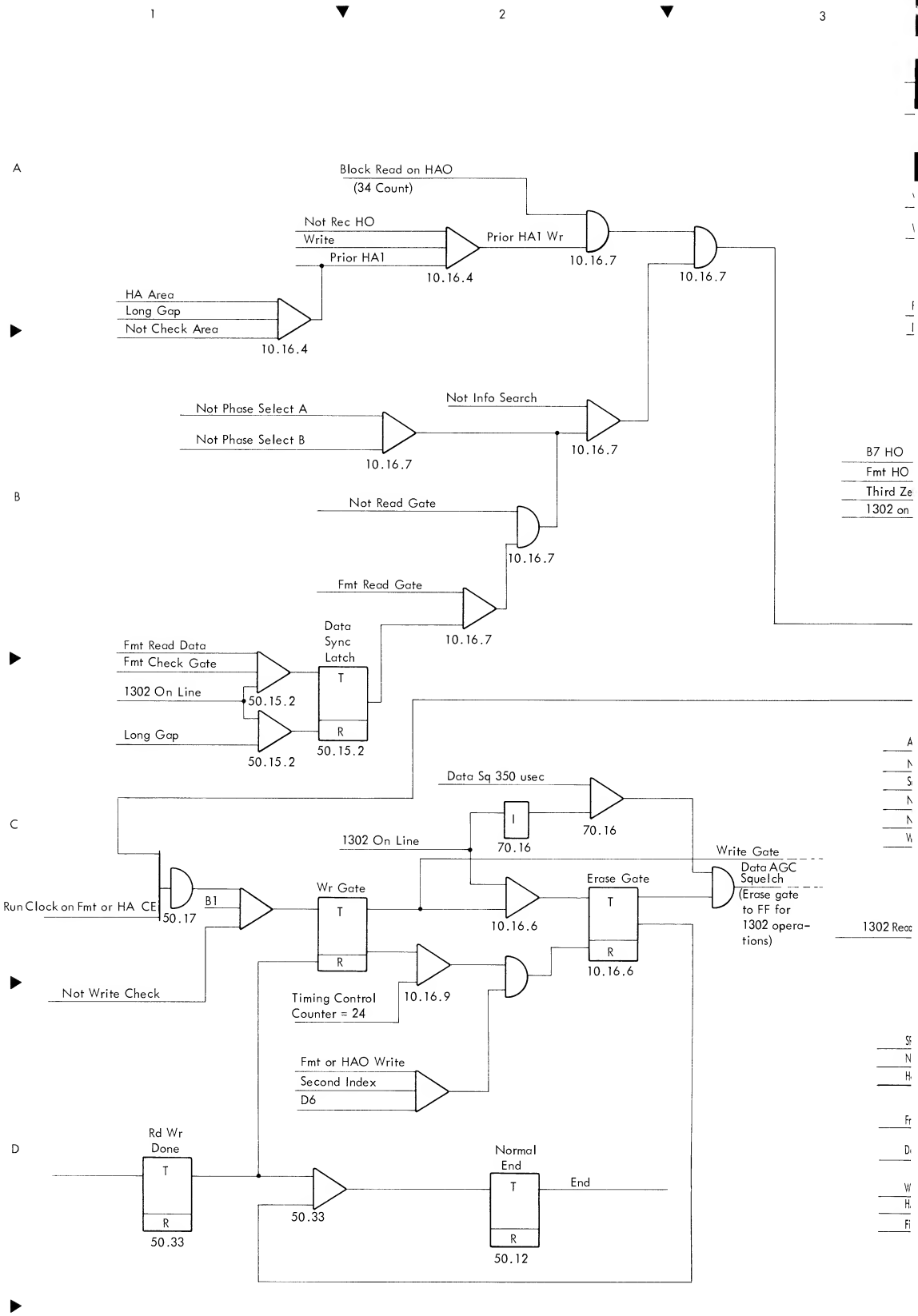
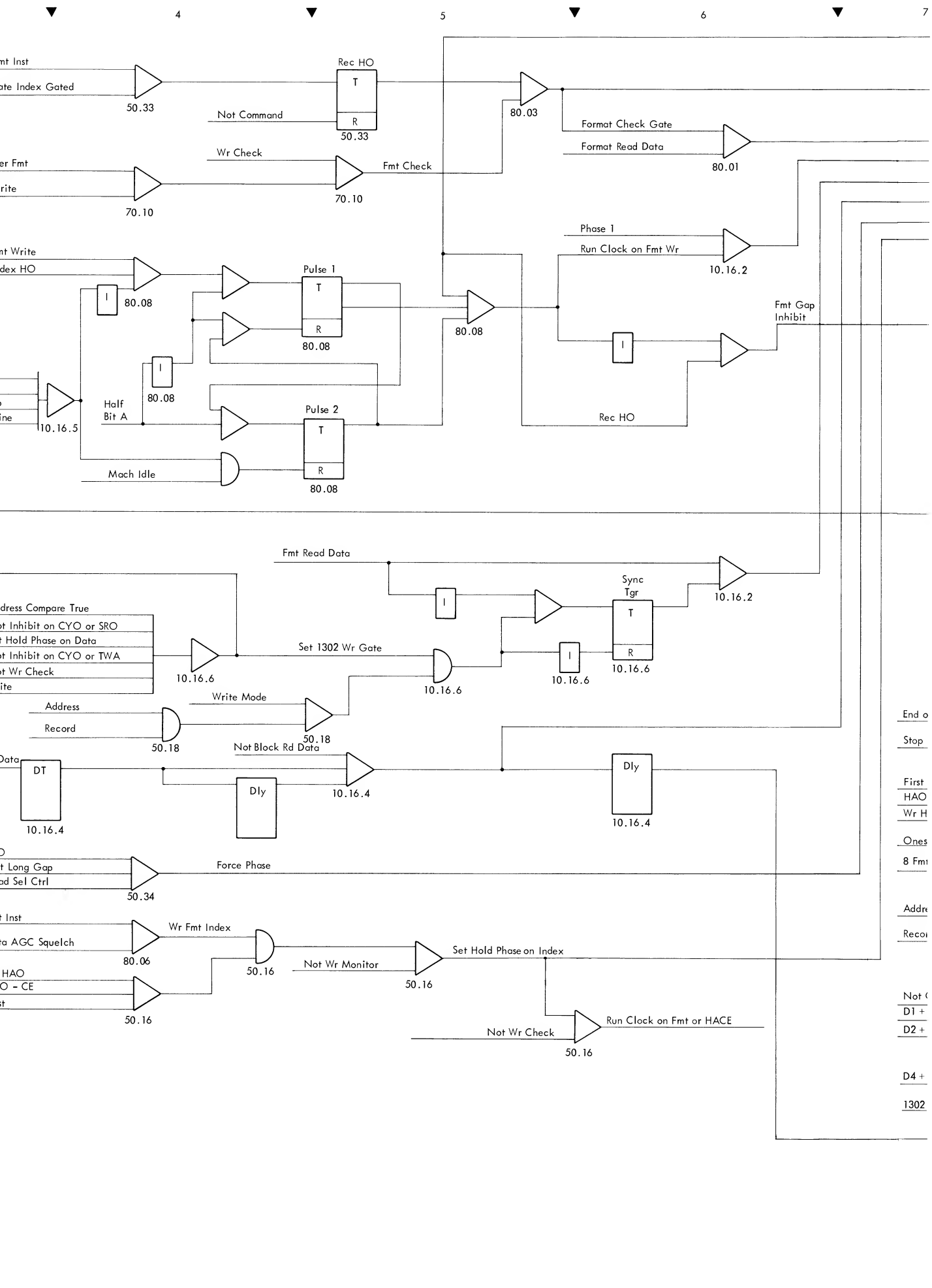
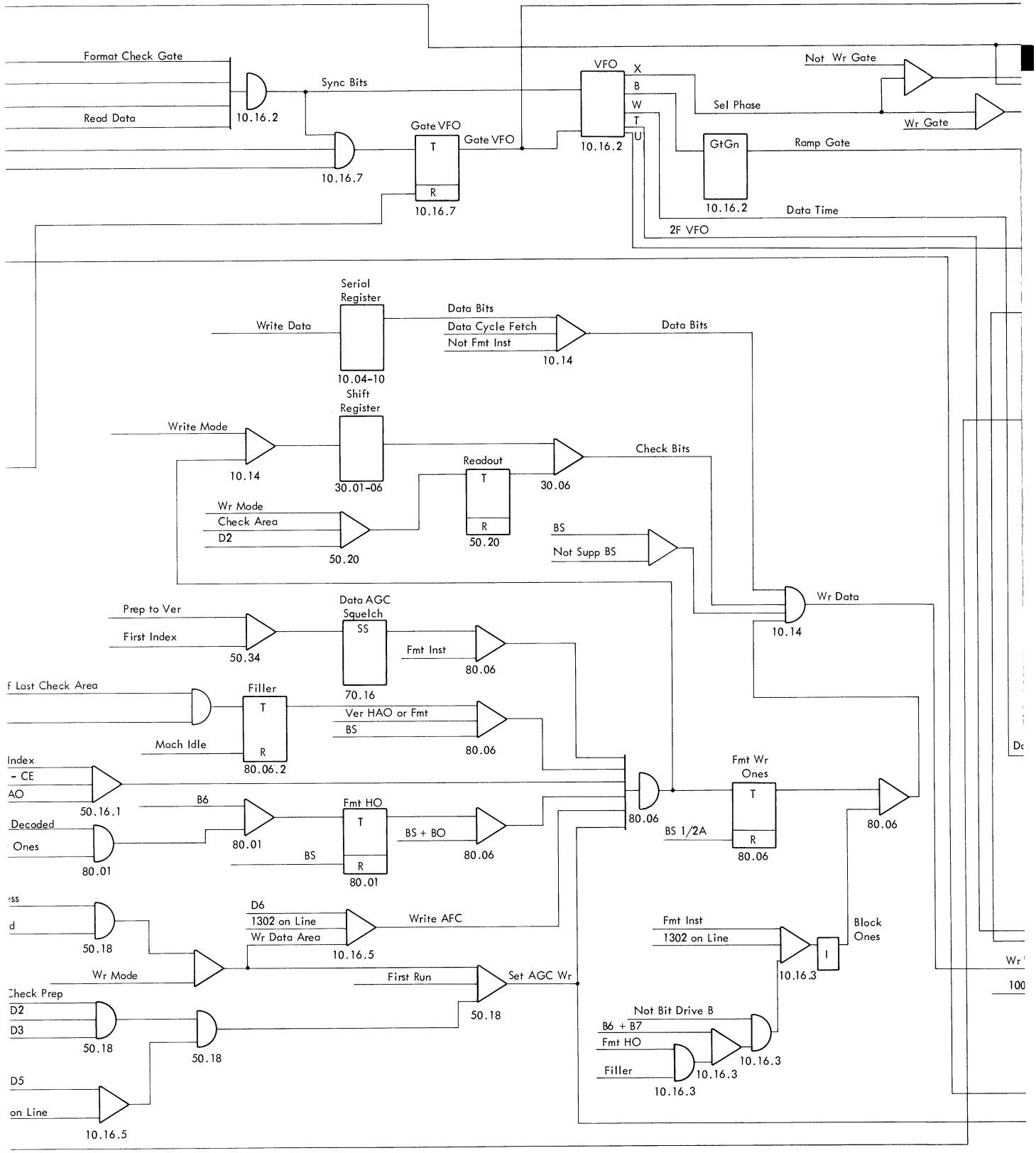
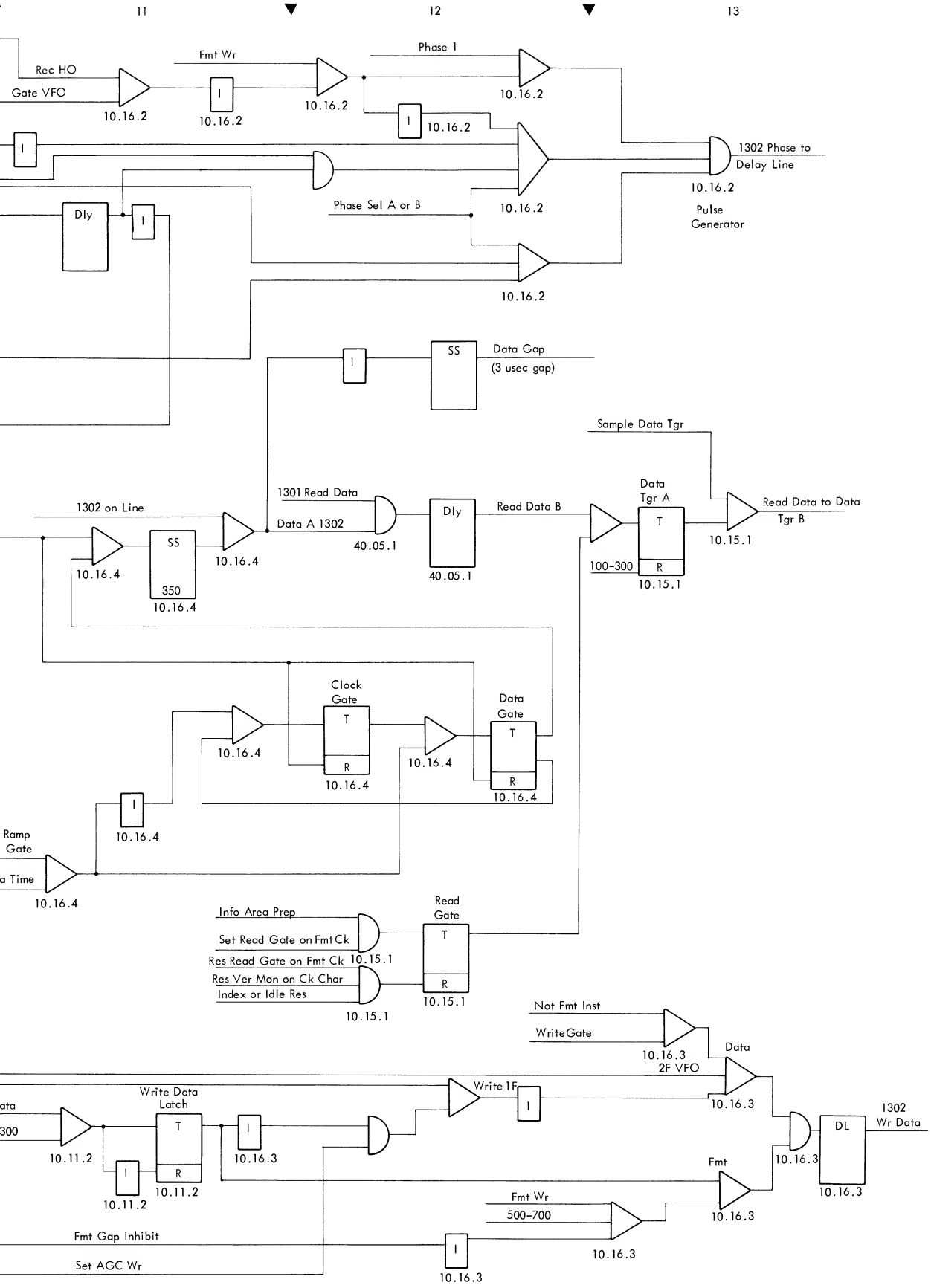


Figure 16. 7631-1302 Operations


4
5
6
7
Rec HO
T
R
50.33
Not Command
80.03
Format Check Gate
Format Read Data
80.01
Wr Check
Fmt Check
70.10
Phase 1
Run Clock on Fmt Wr
10.16.2
Pulse 1
80.08
Fmt Gap Inhibit
Half Bit A
Pulse 2
Rec HO
10.16.5
Mach Idle
Fmt Read Data
Sync Tgr
Address Compare True
Set 1302 Wr Gate
10.16.6
Write Mode
Address
Record
50.18
Not Block Rd Data
DT
Dly
10.16.4
Force Phase
50.34
Wr Fmt Index
80.06
50.16
Not Wr Monitor
Set Hold Phase on Index
Not Wr Check
Run Clock on Fmt or HACE
End o
Stop
First
HAO
Wr H
Ones
8 Fmt
Addr
Recor
Not (
D1 +
D2 +
D4 +
1302


Format Check Gate
Read Data
10.16.2
Sync Bits
10.16.7
Gate VFO
T
R
10.16.7
Gate VFO
VFO
X
B
W
T
U
10.16.2
Sel Phase
Not Wr Gate
Wr Gate
GtGn
10.16.2
Ramp Gate
Data Time
2F VFO
Serial Register
Write Data
10.04-10
Data Bits
Data Cycle Fetch
Not Fmt Inst
10.14
Data Bits
Shift Register
Write Mode
10.14
30.01-06
Readout
T
R
50.20
30.06
Check Bits
Wr Mode
Check Area
D2
50.20
BS
Not Supp BS
Wr Data
10.14
Prep to Ver
First Index
50.34
Data AGC Squelch
SS
70.16
Fmt Inst
80.06
f Last Check Area
Filler
T
R
80.06.2
Ver HAO or Fmt
BS
80.06
Mach Idle
Index
- CE
AO
50.16.1
B6
Decoded
Ones
80.01
80.01
Fmt HO
T
R
80.01
BS
BS + BO
80.06
80.06
Fmt Wr Ones
T
R
80.06
BS 1/2A
80.06
ss
d
50.18
D6
1302 on Line
Wr Data Area
10.16.5
Write AFC
Wr Mode
First Run
Set AGC Wr
50.18
Check Prep
D2
D3
50.18
50.18
D5
on Line
10.16.5
Fmt Inst
1302 on Line
10.16.3
Block Ones
Not Bit Drive B
B6 + B7
Fmt HO
Filler
10.16.3
10.16.3
10.16.3


11
12
13
A
B
C
D
Rec HO
Gate VFO
10.16.2
Fmt Wr
I
10.16.2
10.16.2
Phase 1
10.16.2
I
10.16.2
1302 Phase to
Delay Line
10.16.2
Pulse
Generator
Dly
I
Phase Sel A or B
10.16.2
10.16.2
I
SS
Data Gap
(3 usec gap)
Sample Data Tgr
1302 on Line
1301 Read Data
Data A 1302
40.05.1
Dly
40.05.1
Read Data B
Data
Tgr A
T
R
100-300
10.15.1
Read Data to Data
Tgr B
10.15.1
10.16.4
SS
350
10.16.4
10.16.4
Clock
Gate
T
R
10.16.4
10.16.4
Data
Gate
T
R
10.16.4
I
10.16.4
Ramp
Gate
a Time
10.16.4
Info Area Prep
Set Read Gate on Fmt Ck
Res Read Gate on Fmt Ck
Res Ver Mon on Ck Char
Index or Idle Res
10.15.1
10.15.1
Read
Gate
T
R
10.15.1
Not Fmt Inst
Write Gate
10.16.3
2F VFO
Data
10.16.3
Write 1F
I
Write Data
Latch
T
R
ata
300
10.11.2
I
10.11.2
10.11.2
I
10.16.3
Fmt
10.16.3
DL
10.16.3
1302
Wr Data
10.16.3
Fmt Wr
500-700
10.16.3
Fmt Gap Inhibit
Set AGC Wr
I
10.16.3

4. Gate VFO and record holdover signals block the phase one selected phase (Figure 16, Area 12A; Figure 17, Line 13).

5. Gate VFO and record holdover signals gate the VFO pin X output onto the selected phase line (Figure 16, Area 12A; Figure 17, Line 13).

6. The clock trigger is set to run the bit ring. Bit ring timing is needed for service requests and data strobes. Bit ring timing also sequences write data from the decoder output to the format holdover trigger, to the format write ones trigger and on to the write data latch (Figure 16, Areas 8D through 12D).

7. The format gap inhibit line is conditioned by run clock on format write to permit format data writing when the record holdover trigger is set (Figure 16, Area 12D).

The start of the previous seven-step sequence is delayed 3.2 microseconds by the pulse one and pulse two triggers (Figure 16, Area 4B). The delay between late index and rise of run clock on format write creates a short gap between the late index and the first format data character. The short gap allows for index jitter. Index jitter can cause late index to overlap a few data bits, if late index arrives slightly late on a subsequent format write check operation. The pulse one and pulse two triggers delay the rise of run clock on format write; this delay holds the write circuits off and the bit ring inoperative. Figure 16 (Areas 4B and 5B) shows how pulse one and pulse two triggers control run clock on format write. Figure 19 (Lines 4 through 8) shows how the pulse one and pulse two triggers delay the rise of run clock on format write (Line 9) for 3.2 microseconds.

The transition from clock track phase one to the VFO selected phase is also made during the late index write delay. Figure 19 (Line 2) shows where gate VFO rises; Line A shows where the selected phase changes. Because the 1302 read amplifiers cannot read a signal that exceeds 640 kc, every other format write data bit is suppressed when writing format data with the VFO. The VFO selected phase is twice the 1302 format read amplifier's upper limit frequency; therefore, if every other format write data bit is suppressed, the writing frequency remains 640 kc. Figure 19 (Line 1) shows the clock track and VFO selected phase timing.

The circuits used to write ½F format data block the format write ones trigger output on every even-numbered bit time. The block ones signal (Figure 16, Area 10D), not bit drive B, and B6 + B7, suppresses writing B0, B2, B4, B6, and B7. Figure 20 shows block ones (Line 13) causes the write data latch (Line 9) to reset on every other bit time. The block ones circuit operation is inhibited when the filler or format holdover trigger is reset; this allows writing the last B7 prior to a format track gap. The B7 data bit is needed to insure that the short and long gap singleshots time out correctly when format read data is used for the format recognition circuits. Figure 20, (Line 12) shows the last character written prior to a gap contains a B7 data bit.

The run clock on format write signal serves one more special purpose when writing format track long gaps. The run clock signal is reset for one bit time at the end of each long gap to extend the gap one bit time; one extra zero bit is written to extend the gap. The extra gap length is needed to reset the VFO when format write checking. The circuits that control run clock on format write are shown on Figure 16 (Areas 4B and 5B). B7HO, format holdover, and the third zero trigger output are used to find the end of a long gap. The end of a long gap resets the pulse two trigger and drops run clock on format write. Figure 19 (Area B, Line 9) shows the conditions that drop run clock on format write. The bit timing at the top of Figure 19 shows that the duration of BS is 1.6 microseconds. The three zeros triggers are used to detect long gap writing. These triggers reset whenever the format write ones trigger is set; therefore, they can be used to determine that a long gap is being written. The format holdover trigger is set prior to writing ones; therefore, it is used to locate the end of a gap (Figure 19, Line 13).

Format writing continues until the computer issues stop. The end sequence for 1302 operation is the same as for the 1301 with two exceptions. When the record holdover trigger is reset, the VFO resets; clock track phase one is gated with not record holdover to complete the format write operation (Figure 17, Lines 6, 10, and 12).

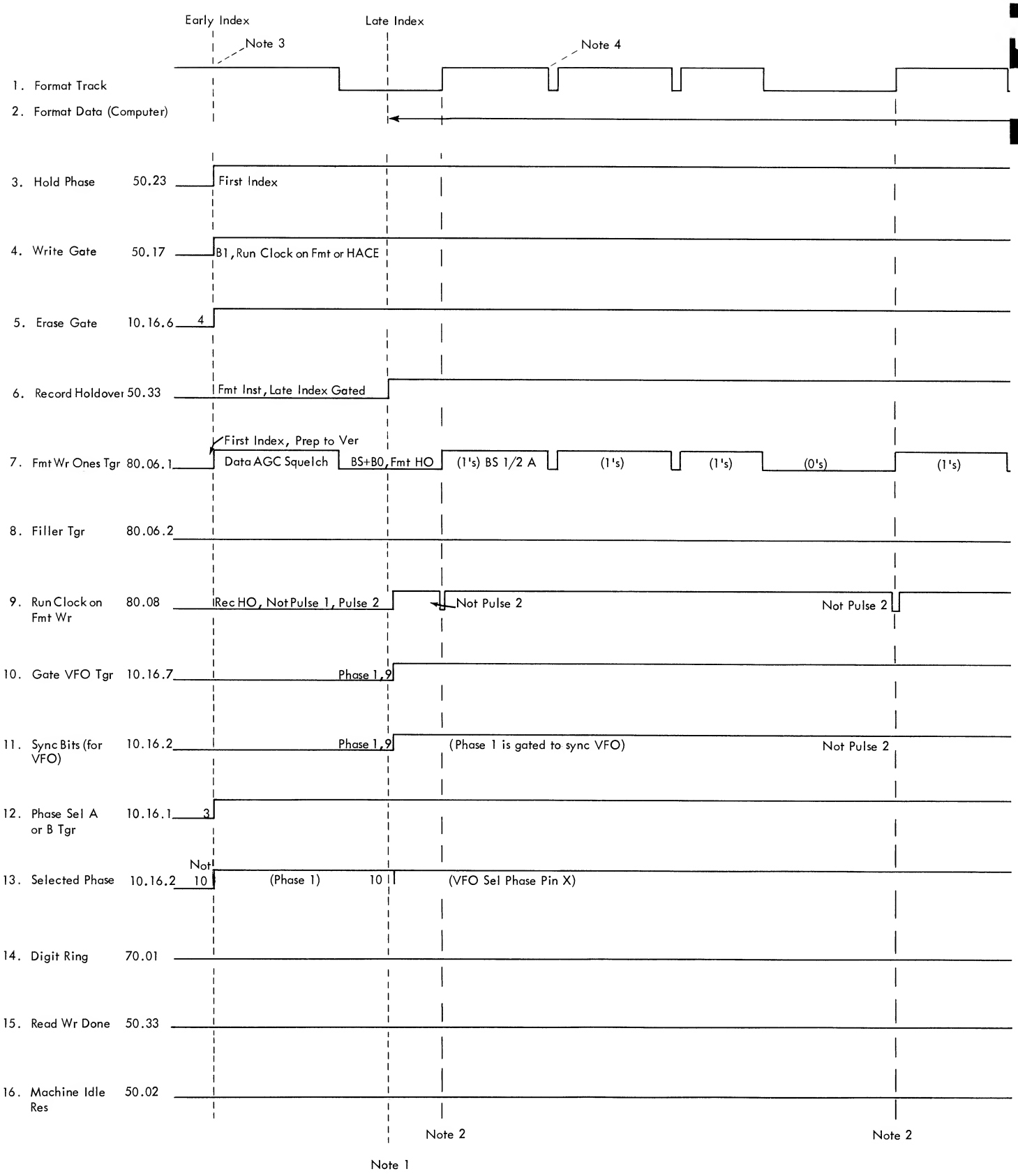
The final exception occurs at the end of the format write operation. D6 of second index is used to reset the erase gate at the same time the write gate drops; this creates a 20 to 38 microsecond unerased area that can be used to adjust heads to read from the track center. Figure 21 (Lines 1 through 5) summarizes the write operation.

HAO-CE Write

The 1302 HAO-CE write timing operation differs from 1301 only during the time the write gate is set. The write operation is divided into two parts:

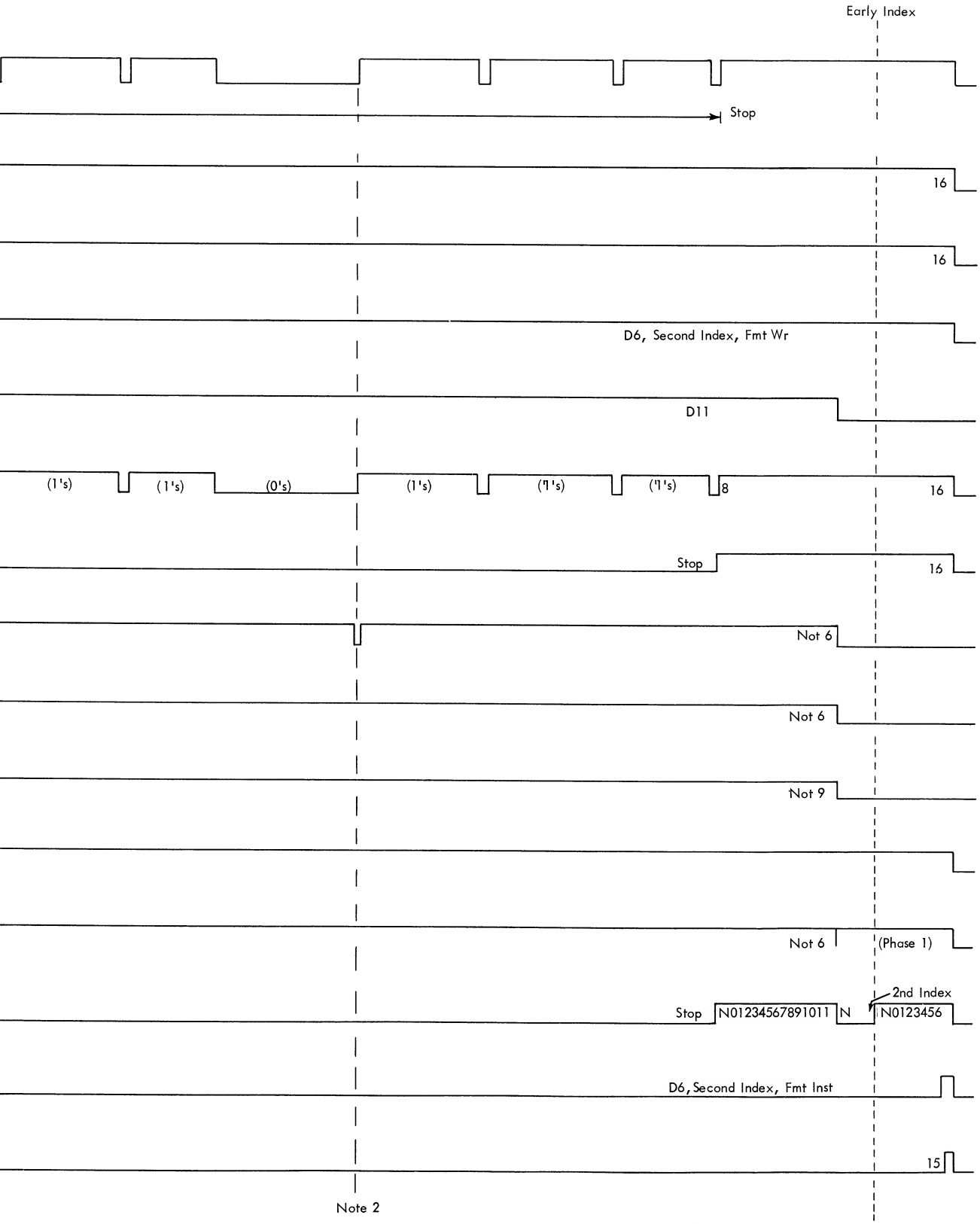
1. Index area writing.
2. Data area writing.

The index area is written with filler bits from early to late index. The index area write timing is supplied by the VFO while it free runs. The irregular spot in the clock track index area prohibits its use as a VFO sync input. Data areas are also written using the VFO as the write timing source. Format read data is used to sync the VFO when writing data.



Note 1. Late index write delay and change from Phase 1 to VFO timing are shown in expanded form on Figure 19, Area A.

Figure 17. Format Write Timing



Note 2. End of long gap delay is shown in expanded form on Figure 19, Area B.
Note 3. Writing filler with phase one is shown in expanded form on Figure 18.
Note 4. Writing format system data (1F) with the VFO is shown expanded on Figure 20.

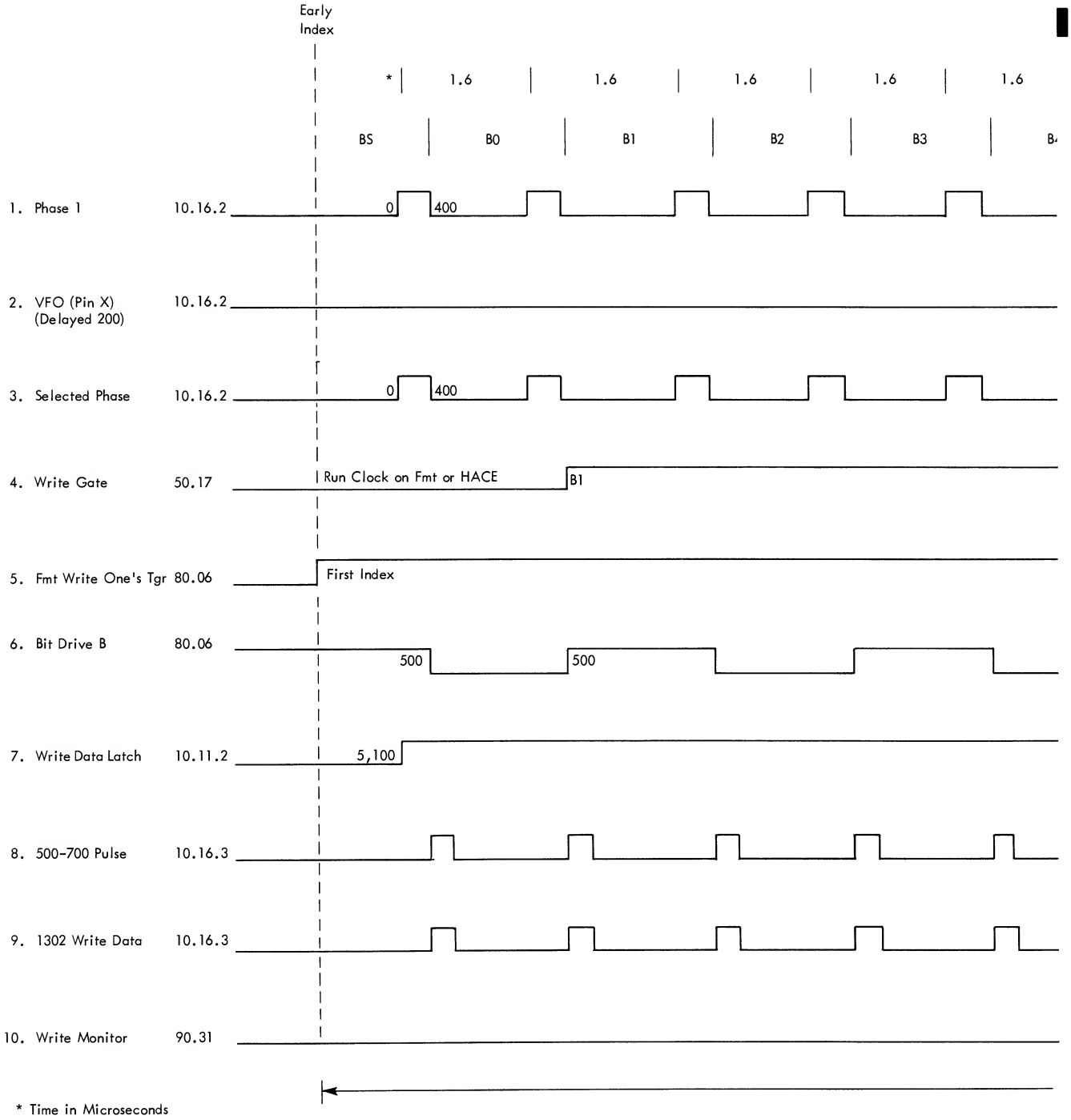
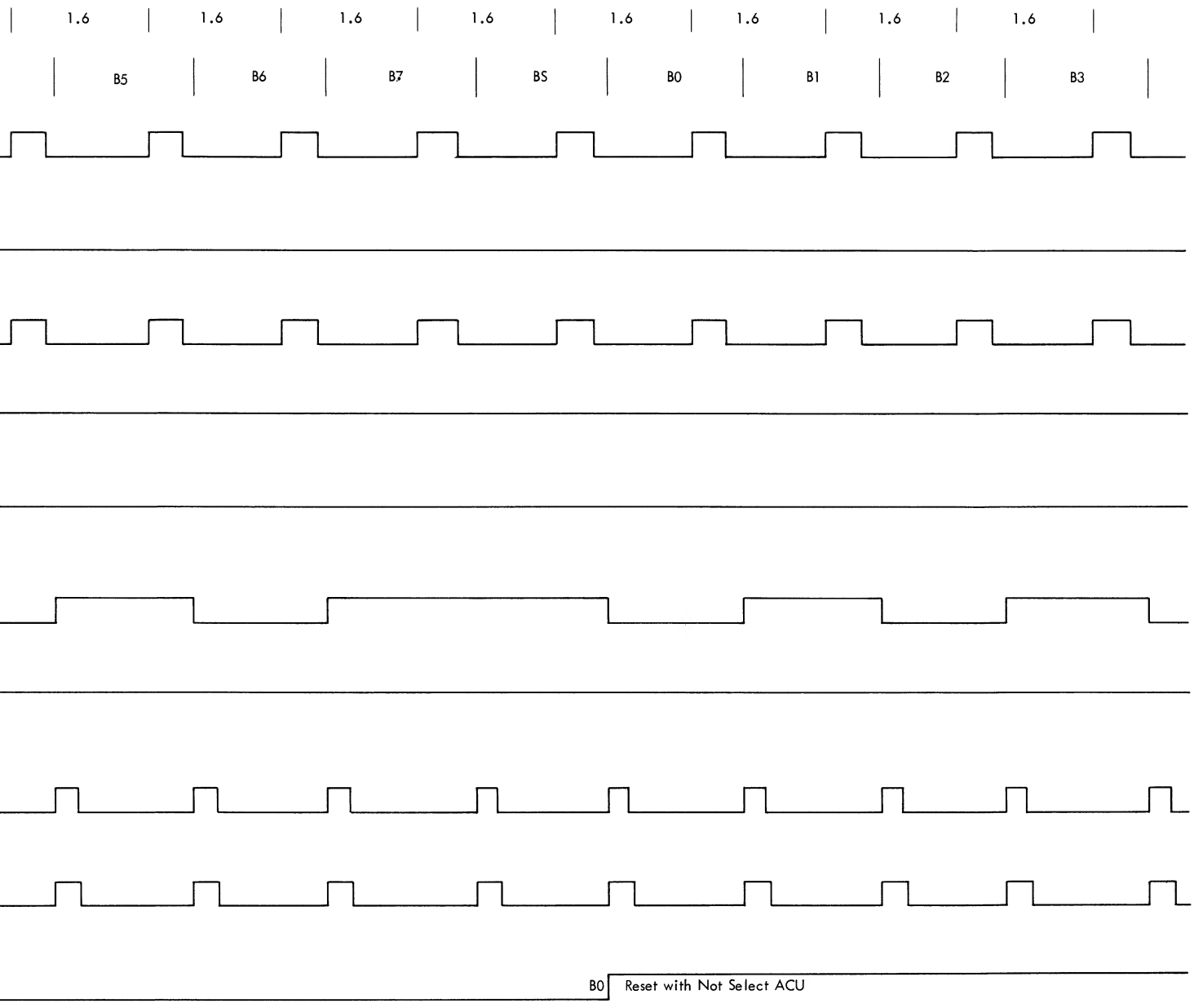


Figure 18. Format Write—Index Area Filler


1.6
1.6
1.6
1.6
1.6
1.6
1.6
1.6
B5
B6
B7
BS
B0
B1
B2
B3
B0
Reset with Not Select ACU
Index Area Filler

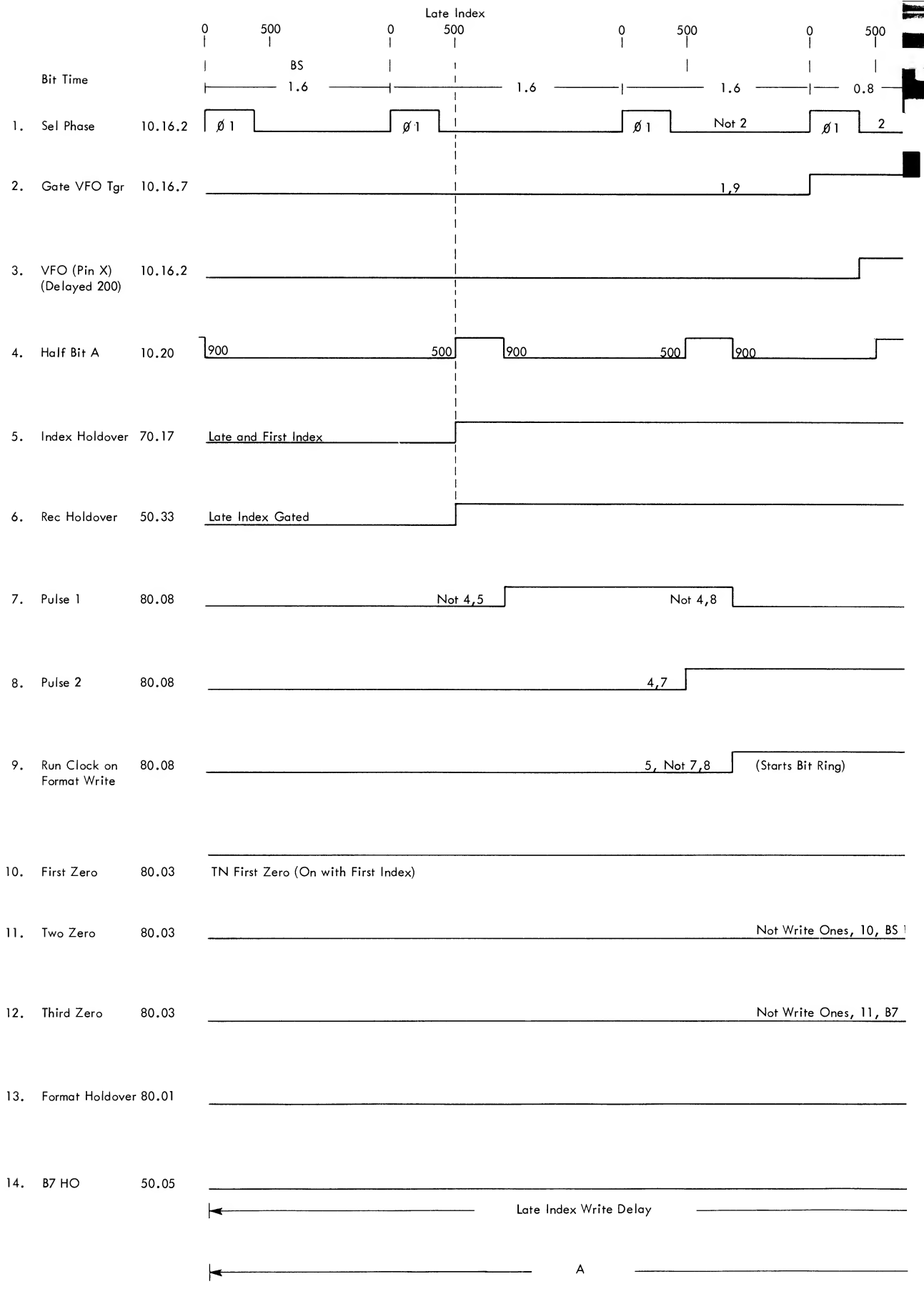
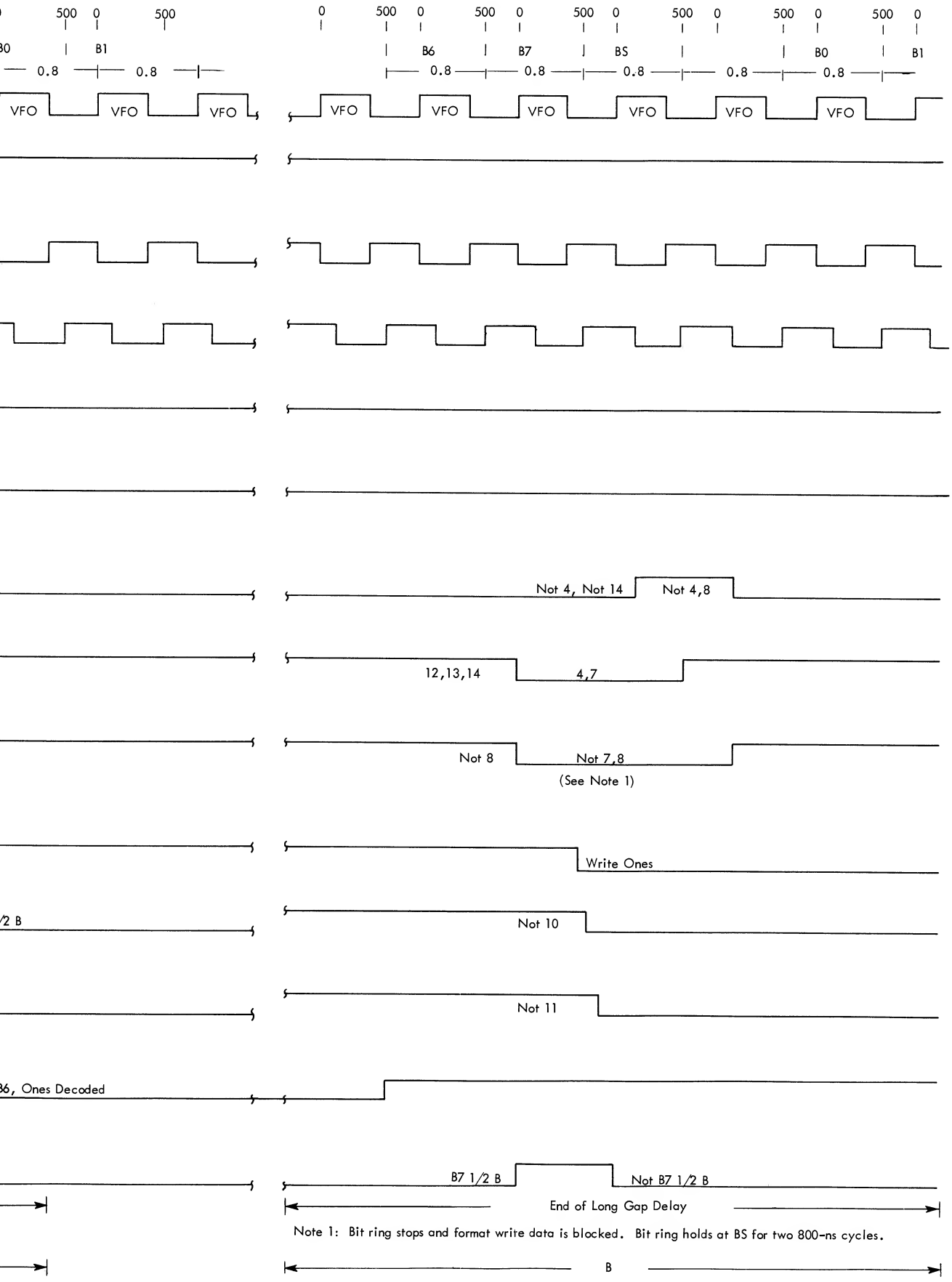


Figure 19. Format Write—Late Index and End of Long Gap Delay



Note 1: Bit ring stops and format write data is blocked. Bit ring holds at BS for two 800-ns cycles.

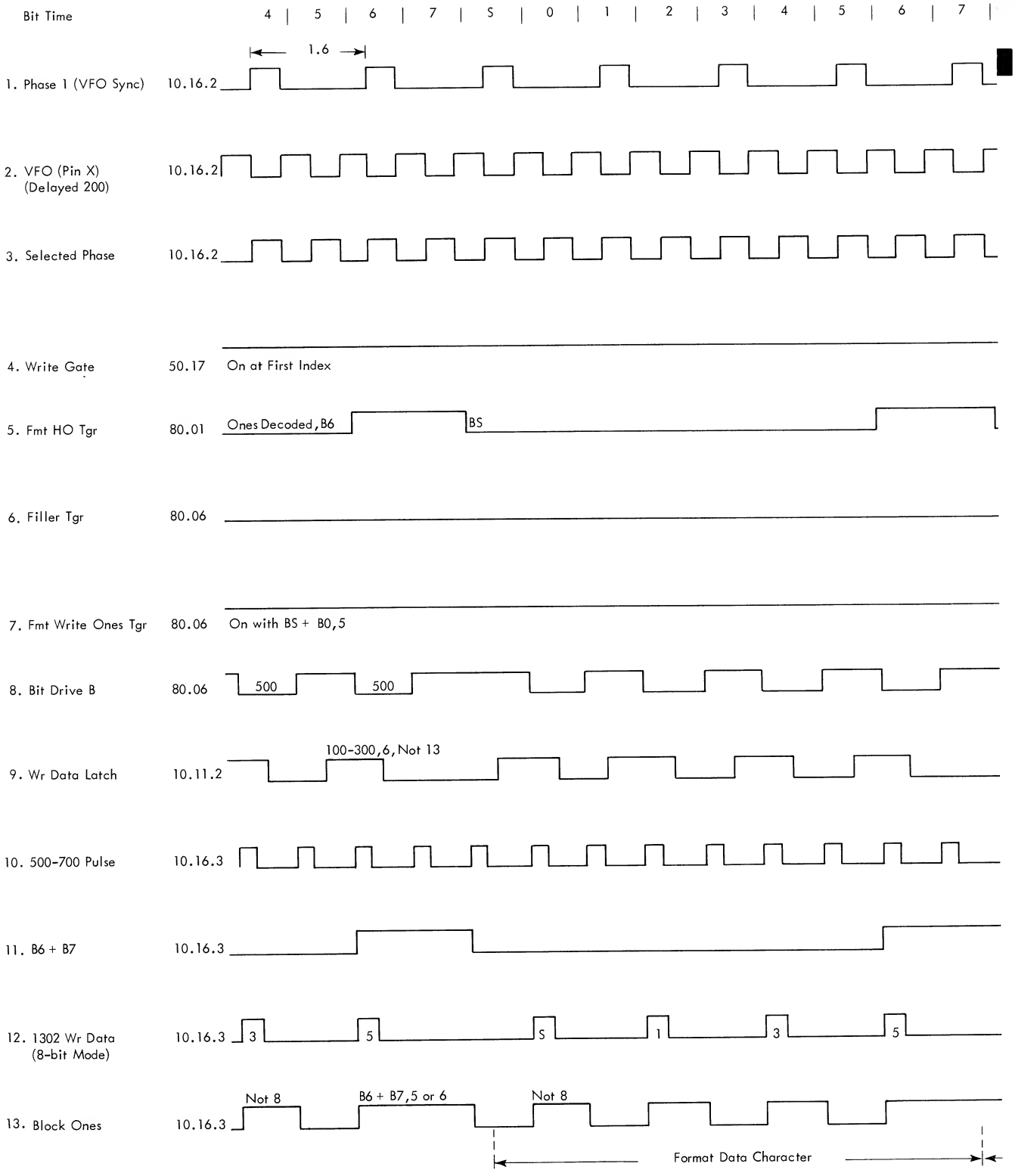
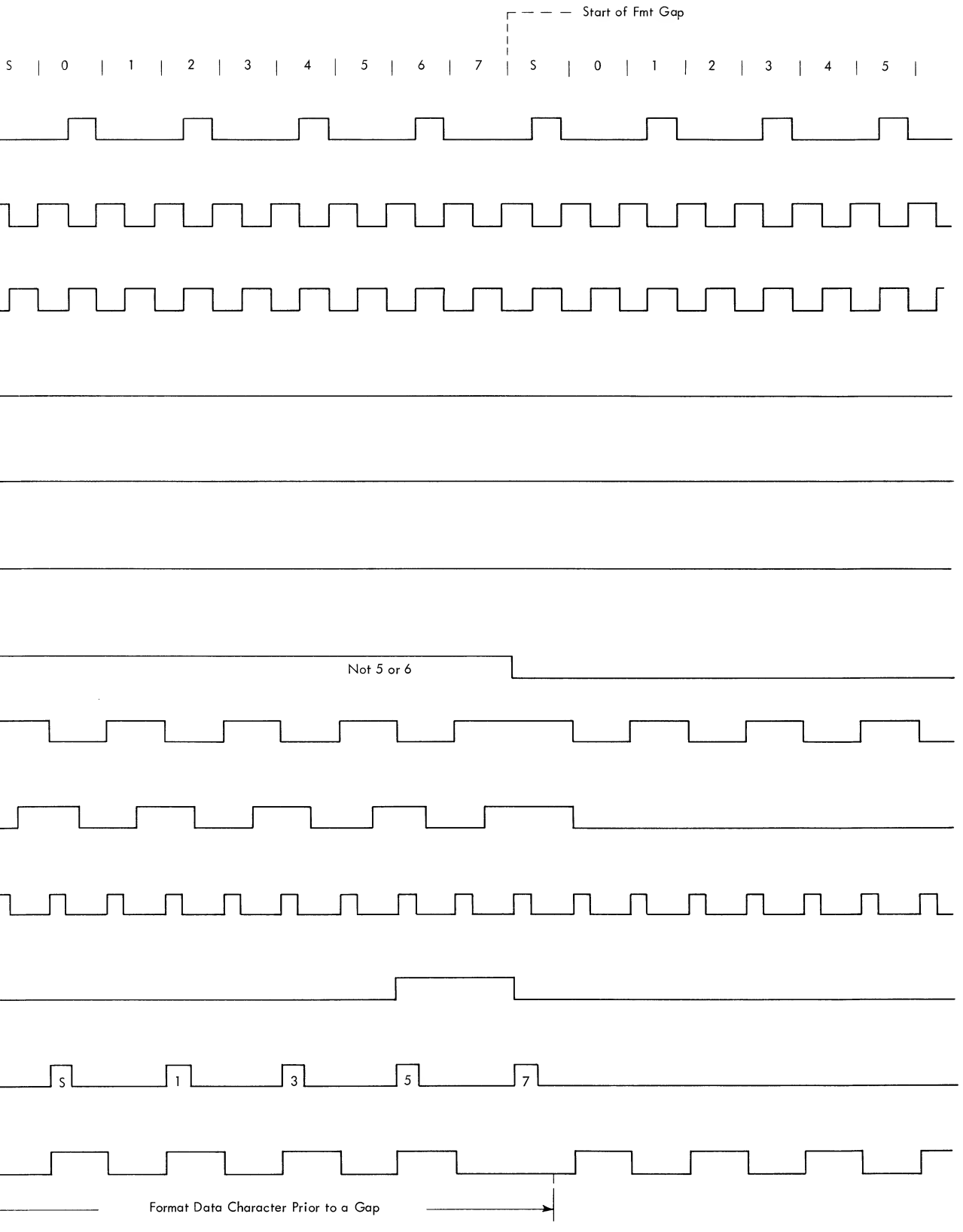


Figure 20. Format Write–Data


Start of Fmt Gap
S | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | S | 0 | 1 | 2 | 3 | 4 | 5 |
Not 5 or 6
S
1
3
5
7
Format Data Character Prior to a Gap

	Operation	Area	Write Data Source	Timing Source Phase 1	Timing Source VFO	VFO Sync	Comments
1	Format Write	Index Area (1/2 F)	Fmt Wr Ones Tgr - Set with 350 usec data AGC Squelch SS	X			350 usec of filler bits are written.
2		Late index to stop (1/2 F)	Fmt Wr Ones Tgr - Set when Fmt HO Tgr is set with system data (ones decoded).		X	Phase 1	VFO is gated on when Rec HO Tgr is set at late index.
3		Stop (end of track) to end of first 11 filler characters.	Fmt Wr Ones Tgr - Set when stop sets Filler Tgr		X	Phase 1	Stop-start digit ring. D11 must reset Rec HO Tgr prior to second index to prevent Format (too long) Error.
4		D11 of filler to second index	Fmt Wr Ones - Set since stop set the Filler Tgr	X			If a maximum length format is written, there will not be space to write these filler characters (Figure 7, area R).
5		Second Index to end. End is D6 of second index.	Fmt Wr Ones Tgr - Set since stop. Reset with machine idle.	X			Simultaneous Write and Erase gate reset creates unerased area on track.
6	HAO-CE Write	Index Area (2F)	Fmt Wr Ones Tgr - Set with First Index		X	None	VFO Free Runs
7		Noise Gap	None		Reset		Write Gate current creates noise gap.
8		HA1 AFC (1F)	Set AGC Write		X	Fmt Data	Write DN - D5 Clock Data.
9		HA1 AGC (2F)	D6 and 1302 on Line		X	Fmt Data	Write D6 Clock and Data. Separated data bits condition Data Gap SS when reading.
10		HA1 AFC Data Gap (1F)	None		X	Fmt Data	VFO on and no data source causes clock bit writing. Absence of data bits allows data gap SS to time out, when reading.
11		HA1 (2F)	Serial Register		X	Fmt Data	VFO free runs when check area write mode resets address or record.
12		HA1 Missing Sync Gap (1F) (Same as AFC Data Gap)	None		X	None	VFO free runs. Write clock bits. Missing sync data bit causes Read Mode Check Area.
13		HA1 Check Characters (2F)	Shift Register		X	None	Write Clock and data.
14		AFC - D5 and D6 of Check Area (1F)	None		X	None	Write clock bits to complete Check Area.
15		Sequence repeats for each of the remaining record, check, and address areas.					Repeat sequence starting with noise gap.
16		Filler - from end of last check area to D6 of Second Index (2F)	Fmt Wr Ones Tgr - End last check area sets Filler Tgr. Filler Tgr set Fmt Wr Ones Tgr		X	None	VFO free runs. Clock and data are written.

Figure 21. Write Operation Summary

Index Area

- **Use the free-running VFO for timing.**
- **Write clock and data for index area filler.**

The objectives are to:

1. Free run the VFO in the index area.
2. Gate the selected phase to the delay line pulse generator input.
3. Set the format write ones trigger to write 2F filler from early to late index.
4. Set the write and erase gates.

Index area writing starts when set hold phase on index sets the gate VFO and hold phase triggers (Figure 16, Area 5D). First index and HAO-CE write set the format write ones trigger for the duration of index area writing (Figure 22, Lines 4 and 14). Run clock on format write sets the clock trigger to run the bit ring. When hold phase sets either phase select A or B trigger, all the conditions needed to operate the timing circuits are established. Phase select A or B trigger output and not format write gate the VFO selected phase to the delay line pulse generator; the timing circuits then begin operation (Figure 16, Area 12A). The first B1 and run clock on format or HACE sets the write gate; the write gate sets the erase gate and index area writing starts (Figure 16, Area 1C and 2C). The next B0 sets the write monitor; the write monitor drops run clock on format or HACE. When run clock drops, the clock trigger resets; the bit ring stops at the next BS. Further bit ring time timing is not needed to continue index area writing.

Another important starting condition is the safety circuit operation. Because both the write and erase gates must be on in the 1302 to drop read safety, the 7631 must generate suppress safety check. The suppress safety check signal prevents two file frame circuits checks. Because the erase gate is slow to rise in the 1302, the slow erase gate rise delays the fall of the read safety and the rise of write safety; the suppress safety check and pseudo write safety drum signals prevent the file frame circuit checks (Figure 22, Lines 19 and 20). The duration of both file frame protection signals is controlled by the timing controls counter; the write gate rise causes the timing controls counter to hold the file frame circuit check protection for 16 microseconds. The counter resets suppress safety check after ten phase one pulses are counted.

Index area write data flows from the format write ones trigger to the write data latch and on to the write circuits (Figure 16, Areas 8C to 12D). The format write ones trigger is set when first index, write HAO, and HAO-CE AND (Figure 16, Area 8C). The data write circuits write 2F filler bits in the index area (Figure 16, Area 12D).

The conditions needed to write filler data are:

1. Not format instruction.
2. Write gate.
3. 2F VFO.
4. Not write 1F.

Every 2F VFO pulse gates a write data pulse to the write driver. When the write data latch is set, its output blocks the VFO selected phase and data is written with every 2F VFO pulse (Figure 22, Index Area Filler). Use Figure 21 as a guide to the timing sequence.

Data Area

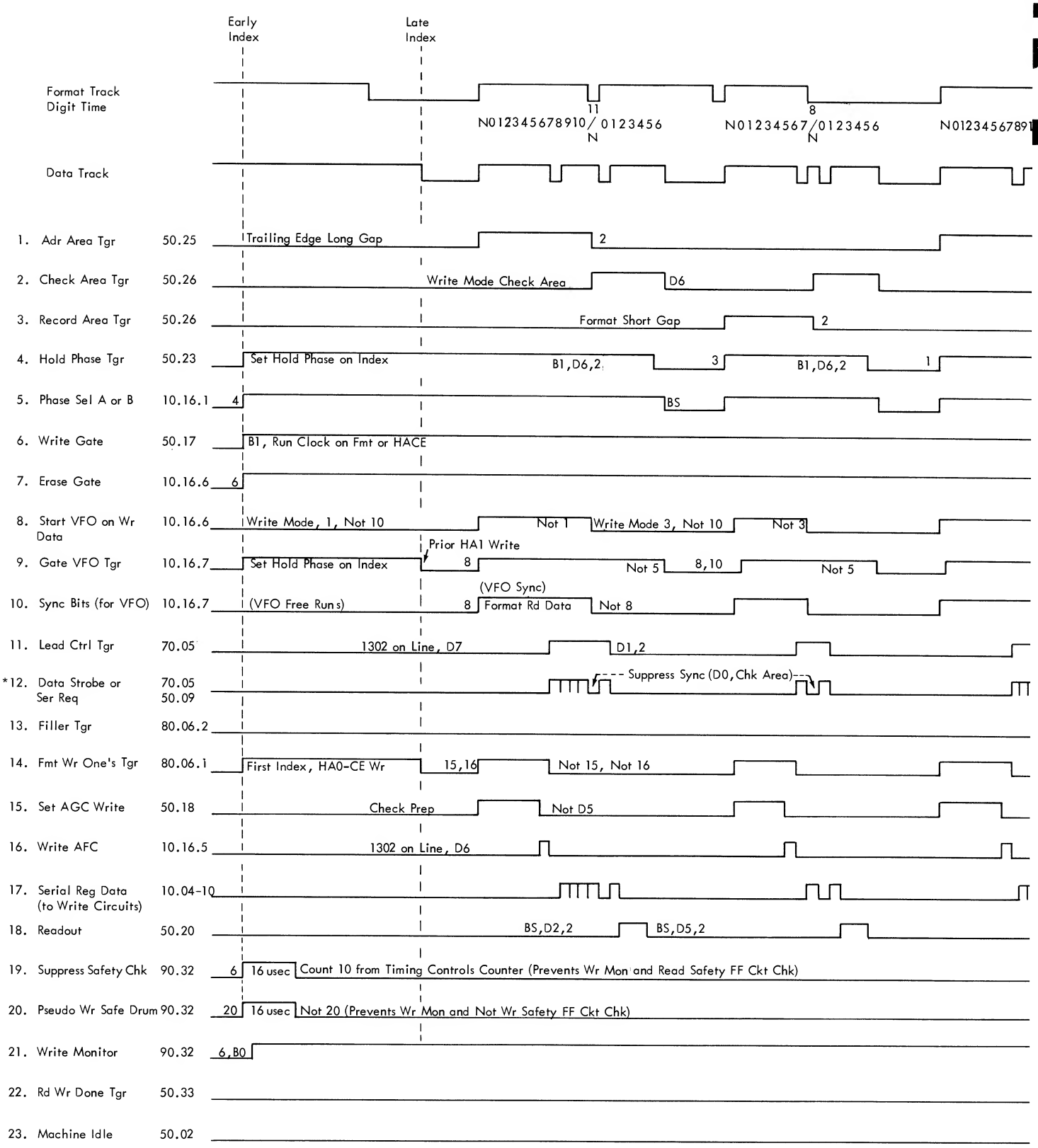
- **Start writing on address or record.**
- **Use the VFO for write timing.**
- **Synchronize VFO with format read data to eliminate skew.**
- **Inhibit skew detector with 1302 on line.**
- **Issue first strobe or service request for data at D7.**
- **Write first data character at D8.**
- **Stop VFO after last AFC character is written.**

The write data objectives are to:

1. Start the VFO with each address or record area.
2. Sync the VFO with format read data during each address and record area to eliminate skew.
3. Inhibit skew detector with 1302 on line.
4. Free run the VFO in each check area.
5. Reset the VFO when check area ends.
6. Gate the selected phase to the delay line pulse generator input.
7. Write data.

The write data sequence starts when write mode and address area signals set the start VFO on write data trigger; format data sets the gate VFO trigger and syncs the VFO (Figure 16, Areas 7A through 9A; Figure 22, Lines 8, 9, and 10). Write timing is available when the VFO starts operating because the conditions needed to gate the selected phase were previously established (Figure 16, Area 12A). Bit and digit ring timing are shown on Figure 23.

Each address or record area must contain seven AFC characters; the AFC characters are needed to sync the VFO in subsequent read operations. Seven AFC characters are written when the VFO timing and set AGC write condition the write data circuits. Figure 16 (Areas 7D and 8D) shows how set AGC write is generated. The data written is 1F because set AGC write conditions the write one 1F control to the write circuits (Figure 16, Area 12D). Figure 24 (Line 8) shows not selected phase and set AGC write block data bit writing and allow only clock bit writing in the AFC area.



* Data strobes occur at B6. Service requests occur at B1 and are three bit times in duration.

Figure 22. HAO-CE Write Timing

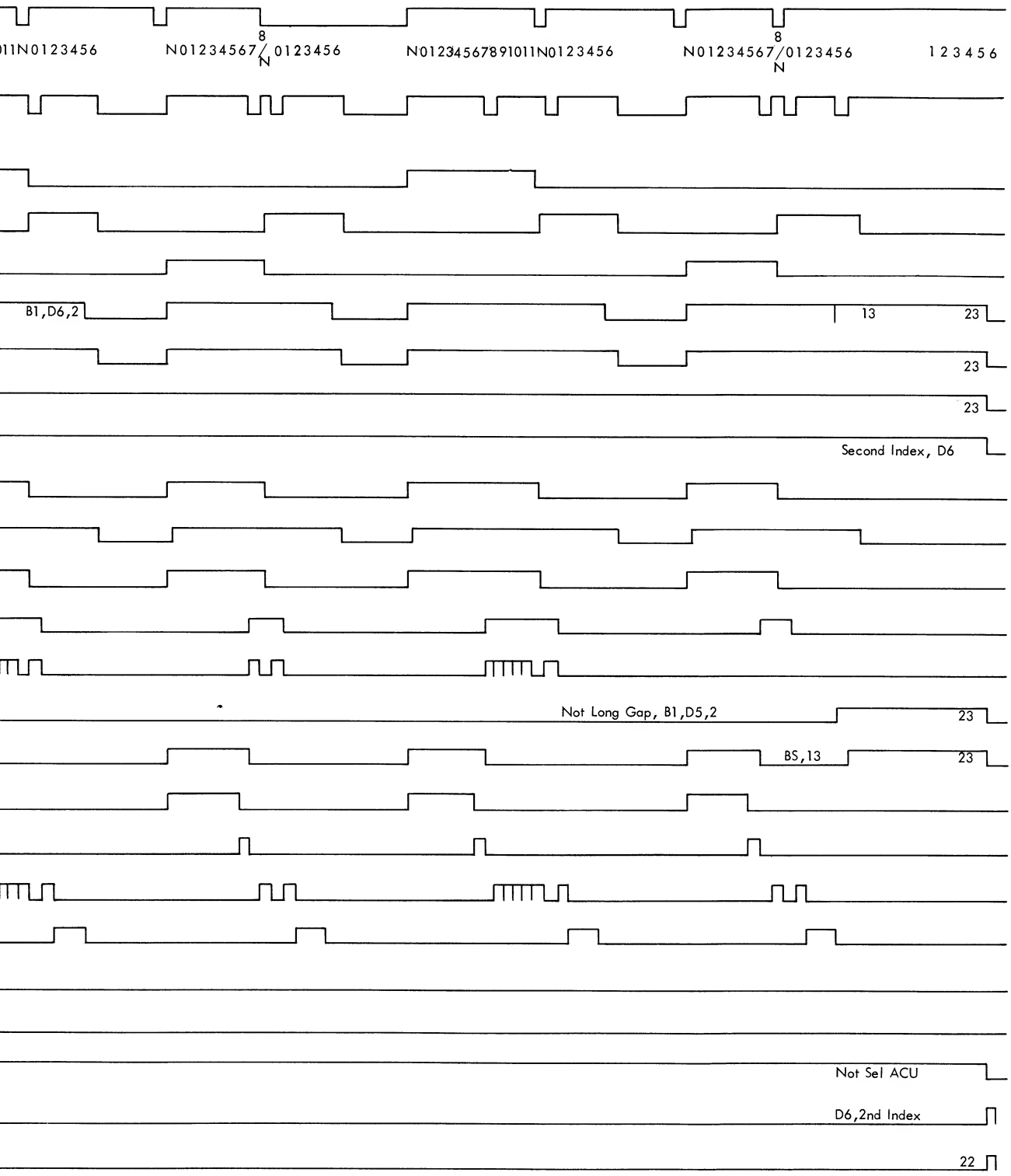

011N0123456
N01234567 8/N 0123456
N01234567891011N0123456
N01234567 8/N 0123456
123456
B1,D6,2
13
23
23
23
Second Index, D6
Not Long Gap, B1,D5,2
23
BS,13
23
Not Sel ACU
D6,2nd Index
22

Figure 24 shows how the AGC character is written adjacent to the last AFC character at D6. The 2F AGC data conditions the data gap singleshot in subsequent read operations. The separated data bits prepare the data gap singleshot to time out in the data gap; this causes the read gate to set. The absence of set AGC write and the inverted output of the write data latch suppress write 1F; this causes 2F writing (Figure 24, Line 8).

Adjacent to the 2F AGC character, one character of clock bits is written to define the data gap. The write 1F control to the write circuits must be active to suppress the data bit writing. The reset write data latch output gates the VFO selected phase to suppress data bit writing (Figure 16, Area 12D). Data gap and AFC writing are similar because both write situations suppress data bit writing.

The data gap is written at D7 for 1302 operation; similar to 1301 operation, the lead control trigger is set while writing the data gap to start the data strobe or service request routine (Figure 22, Line 11). The first strobe or service request is issued one digit time prior to data writing to permit time to transfer the character into the serial register.

Data writing starts at D8 of each address or record area (see digit time at the top of Figure 22). Write data are serially transferred from the serial register to the write data latch with each bit time pulse. Figure 25 shows the write circuit timing while writing a BCD A. The timing shows that whenever the write data latch is reset the write one 1F line blocks data bit writing.

The 1302 write data sequence continues through check area, where the readout gate permits three check characters to be written. Address area trigger resets when the format track short gap sets the check area trigger. The fall of address area resets set 1302 write gate; the fall of set 1302 write gate resets the start VFO on write data trigger (Figure 16, Area 5C). Because the start VFO on write data trigger controls format data to the VFO sync input, the VFO free runs until check area ends at D6 (Figure 22, Lines 8, 9, and 10).

After the check characters are written, the reset write data latch conditions write 1F; two characters of AFC clock bits (with sync bits) are written during D5 and D6 to complete the check area writing. While check area writing is being completed, B1 or D6 resets the hold phase trigger; the absence of hold phase causes the phase select A or B trigger to reset (Figure 22, Lines 4 and 5).

The VFO is clamped off when not info search, not read gate, and not phase select A or B resets the gate VFO trigger (Figure 16, Areas 1B and 2B).

The timing and write circuits remain off from the end of each check area until the next address or record area starts. The absence of write data and the set write gate creates the gap that separates the check characters from the next write data area. Each additional formated write data area is written with an identical sequence (Figure 22). The sequence is repetitive until end of last check area occurs.

The filler trigger is set with end of last check area; end of last check area occurs when record holdover, not long gap, B1, D5, and check area AND. The filler trigger prevents the hold phase trigger from resetting at D6 of the last check area on the data track. When hold phase remains on, the phase select A or B trigger cannot reset; phase select A or B trigger on prevents the gate VFO trigger reset. This sequence, starting when the filler trigger sets, is needed to continue the VFO operation and 2F filler writing until the operation ends at D6 of second index (Figure 22, Lines 4 and 13). The HAO-CE write operation ends when D6 of second index sets the read write done trigger. Digit six of second index resets the erase gate when the write gate resets to create a 20 to 38 microsecond unerased area on the data track.

Read Data

- **Block raw data in noise gaps.**
- **Block first 20 AFC bits (16 μs).**
- **Synchronize VFO on raw read data.**
- **Set read gate during data gap.**
- **Gate separated data to the serial register.**
- **Block raw read data after the read gate resets.**

The 7631-1302 read circuits are a combination of sequence controls and data separation circuits. The sequence controls gate raw read data, stop and start the timing circuits, and control the VFO. The data separation circuits use the VFO timing to separate the data bits from the raw data. The read data objectives are to:

1. Gate raw read data after the noise gap.
2. Gate the VFO.
3. Sync the VFO.
4. Run the bit and digit rings with hold phase timing prior to the data area for gap detection and for a compare circuit test when verifying address.
5. Detect the data gap and gate separated data to data triggers A and B.
6. Assemble read data in the serial register.
7. Reset the read gate at the end of check characters.

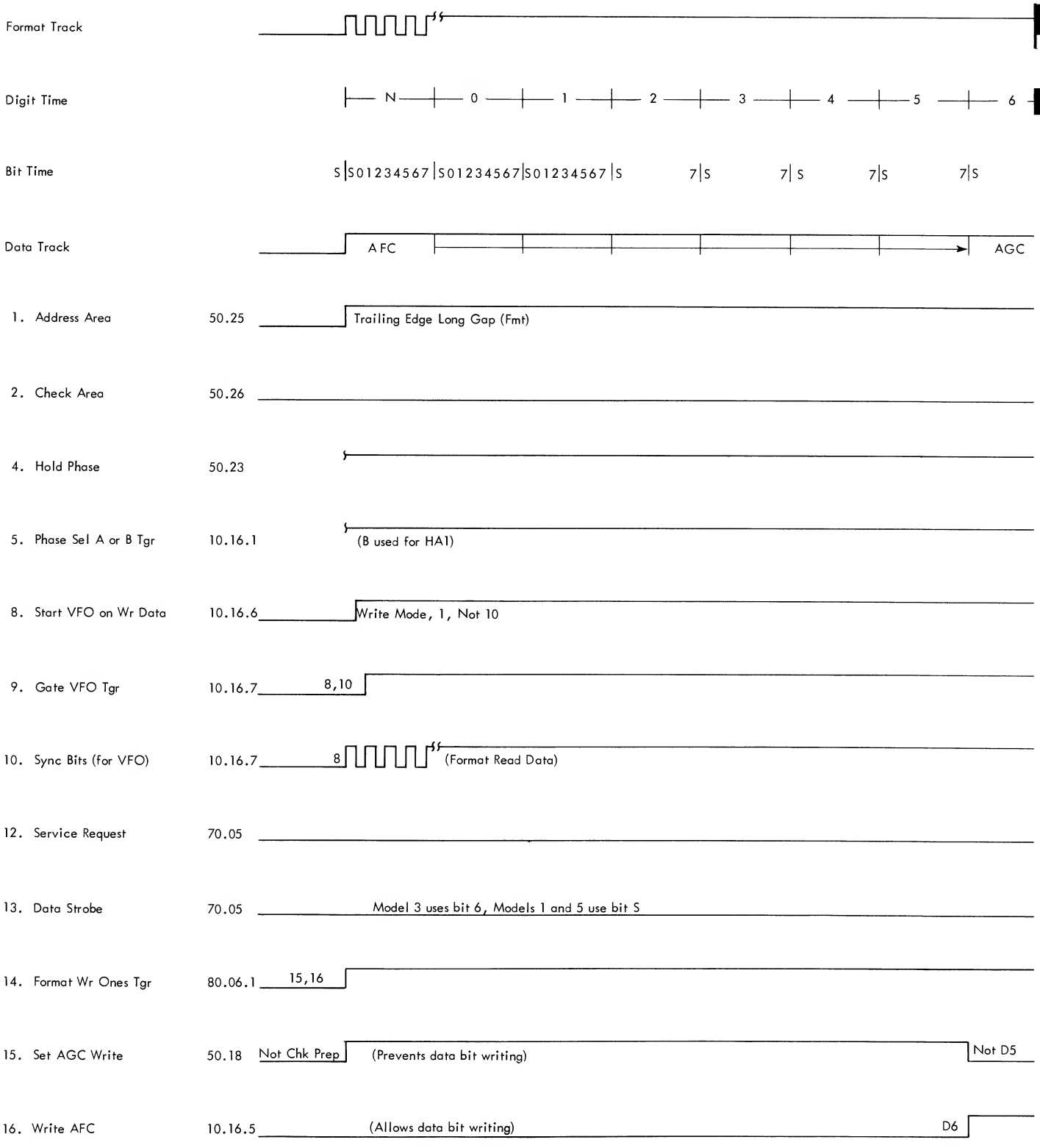
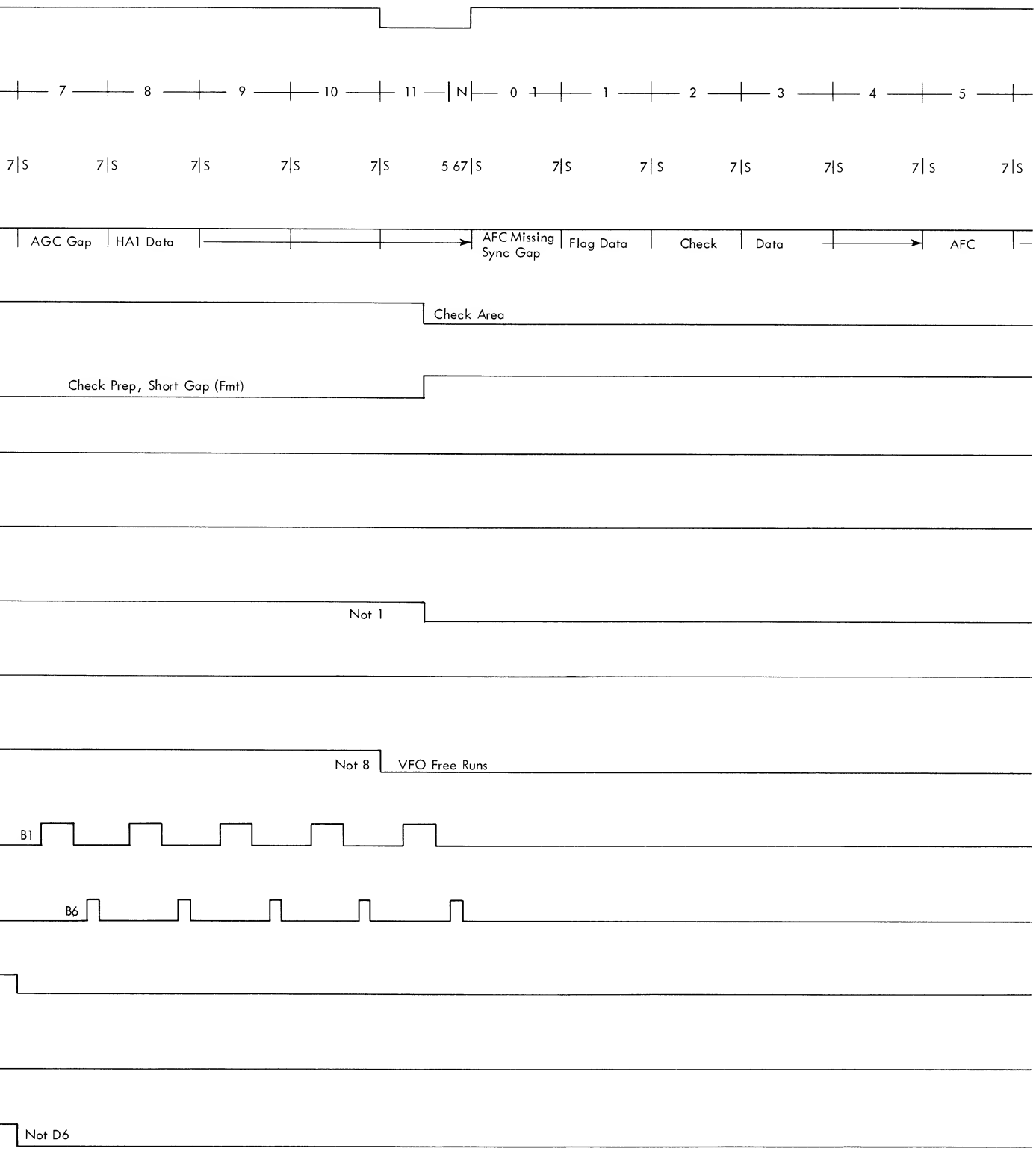
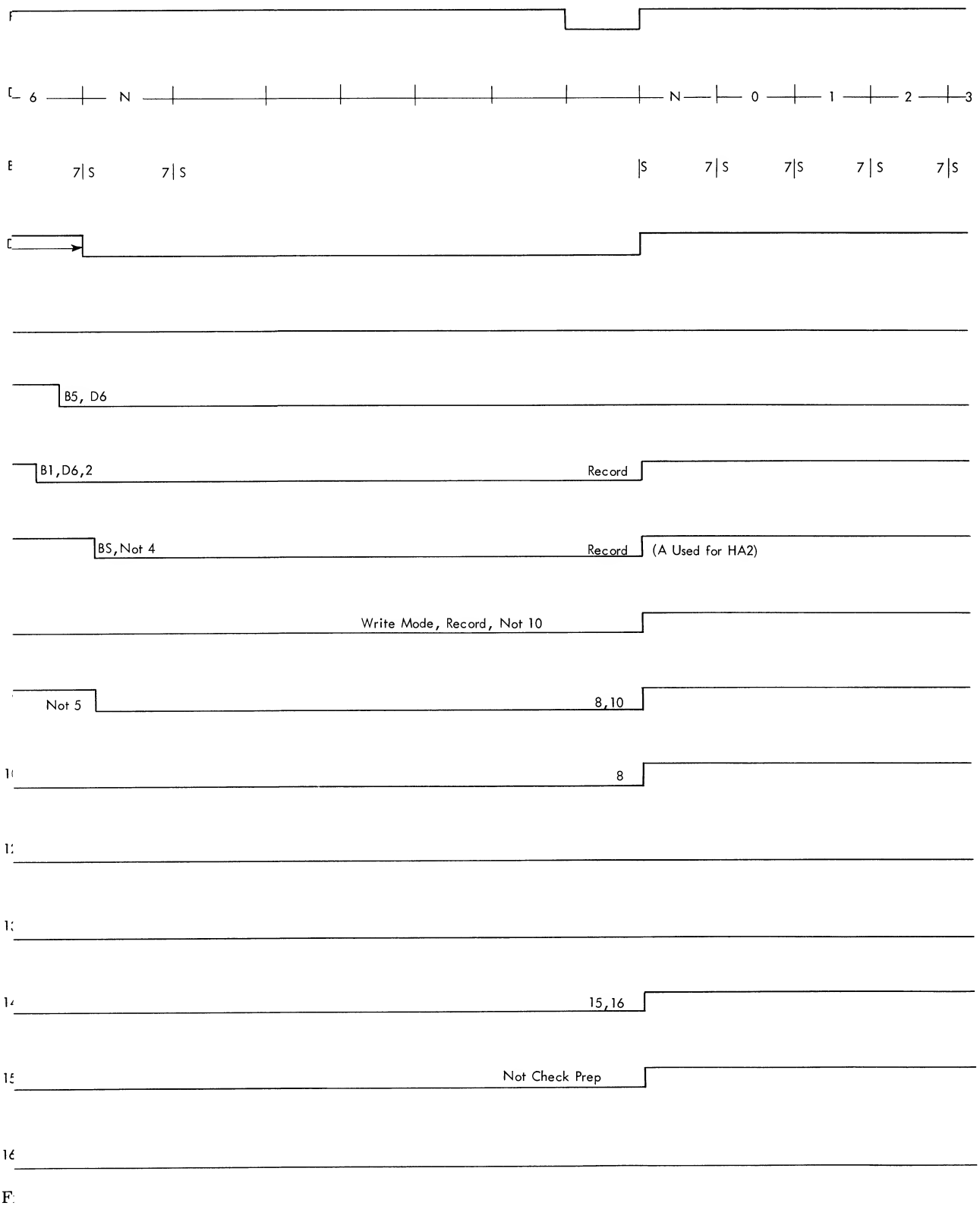
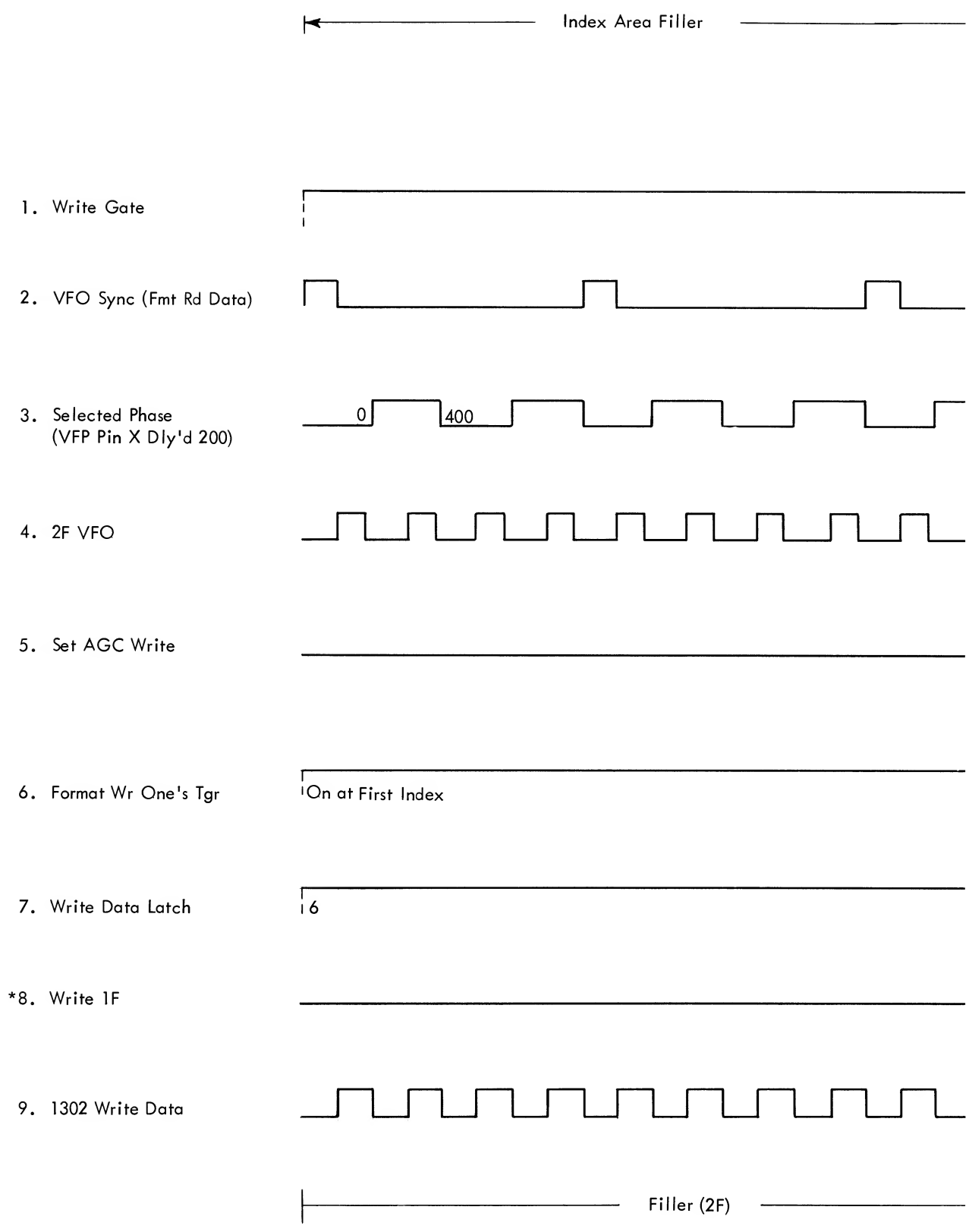


Figure 23. HAO-CE Write Timing—Write HA1—Eight-bit Mode

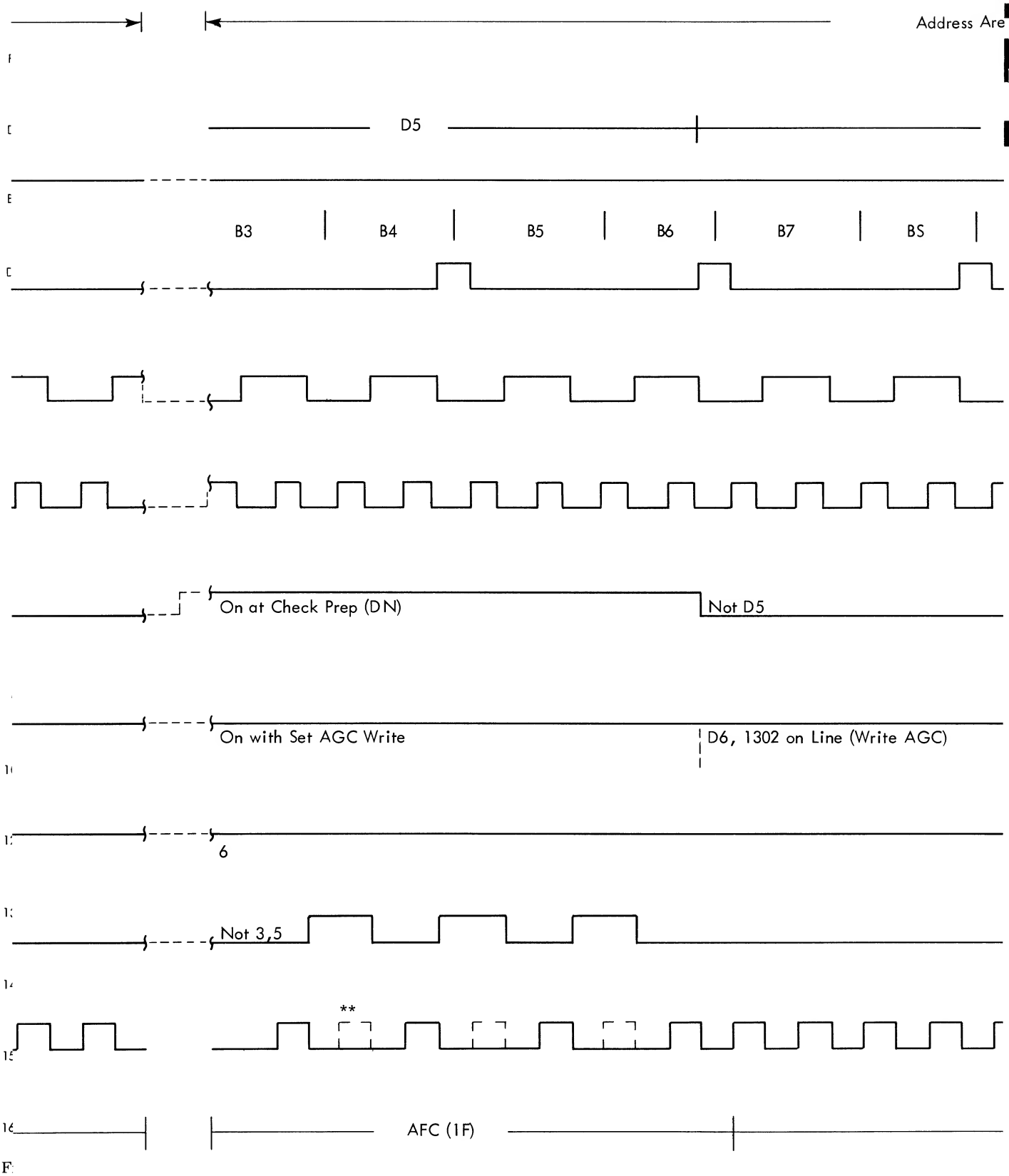

7 8 9 10 11 N 0 1 2 3 4 5
7|S 7|S 7|S 7|S 7|S 5 67|S 7|S 7|S 7|S 7|S 7|S 7|S
AGC Gap
HA1 Data
AFC Missing Sync Gap
Flag Data
Check
Data
AFC
Check Area
Check Prep, Short Gap (Fmt)
Not 1
Not 8
VFO Free Runs
B1
B6
Not D6

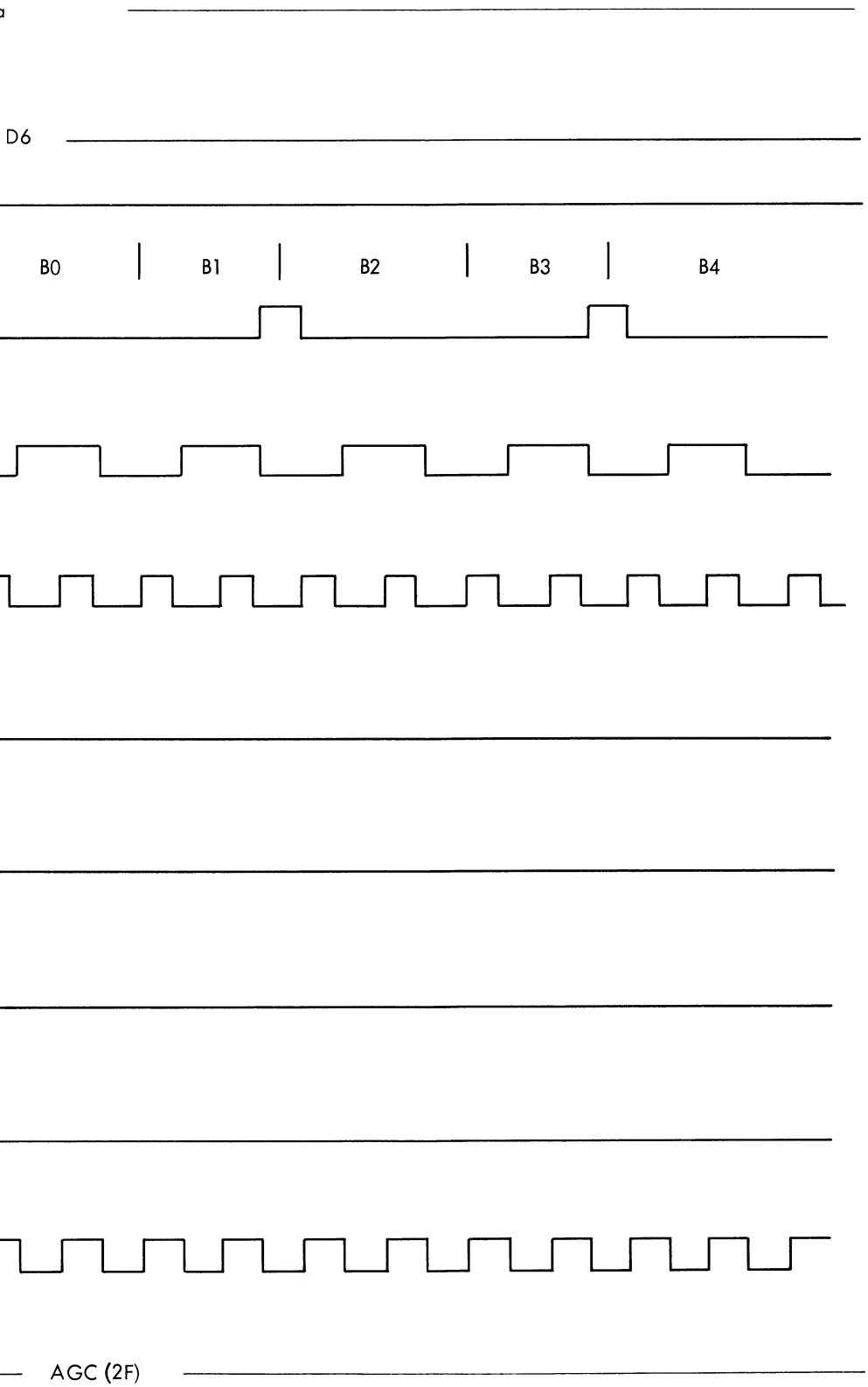

6
N
N
0
1
2
3
7|S
7|S
|S
7|S
7|S
7|S
7|S
B5, D6
B1,D6,2
Record
BS,Not 4
Record
(A Used for HA2)
Write Mode, Record, Not 10
Not 5
8,10
8
15,16
Not Check Prep

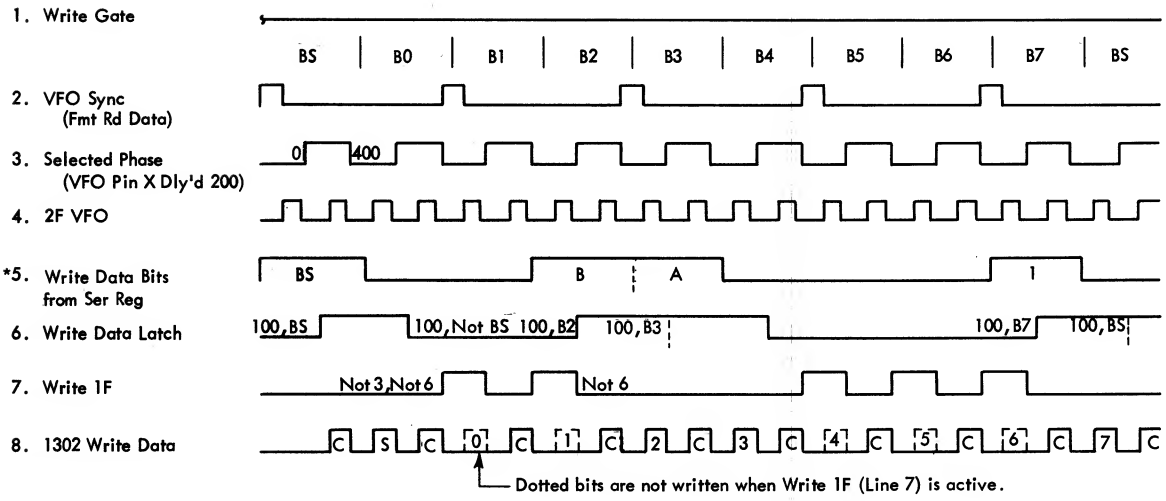


* All bits are written when Write 1F (line 8) is inactive.
** Dotted bits are not written when Write 1F (line 8) is active.

Figure 24. HAO-CE Write Timing—Index, AFC, and AGC Writing


Address Are
D5
B3
B4
B5
B6
B7
BS
On at Check Prep (DN)
Not D5
On with Set AGC Write
D6, 1302 on Line (Write AGC)
6
Not 3,5
**
AFC (1F)


D6
B0
B1
B2
B3
B4
AGC (2F)



* Character is a BCD A

Figure 25. HAO-CE Write Timing—Data

8. Continue bit and digit ring operation with hold phase, after the last check character, to complete check area timing.

9. Reset the VFO at the end of check area.

10. Block raw read data after the last check character until 16 microseconds of the next address or record AFC have passed the read head.

Read Operation

The read operation starts when address or record sets the hold phase trigger; hold phase sets either phase select A or B trigger. Address or record prepares the bit and digit rings to run and also starts the timing controls counter. When ten phase one pulses are counted, block read data drops; raw read data sets the gate VFO trigger and syncs the VFO (Figure 16, Areas 4C and 5C). The VFO selected phase drives the timing circuits to execute the hold phase functions (Figure 26, Lines 4 through 8). The timing circuits stop at BS of D2, when phase select A or B resets (Figure 26, Lines 7 and 8). The AFC bits read prior to the data gap sync the VFO with the data area. (Figure 27 shows bit and digit ring timing.)

When the separated AGC bits are read, the data gap singleshot resets; the absence of data bits in the following gap allows the data gap singleshot to time out and set the read gate (Figure 26, Lines 9 and 10). The read gate controls separated read data flow from the separation circuits to data triggers A and B and on to the serial register (Figure 16, Areas 11B and 12B). The timing circuits resume operation with the first read data bit sync; bit sync sets either phase select A or B trigger (Figure 26, Line 8).

Reading continues until the last check character is read (Figure 26, Line 10). Check area timing sets the hold phase trigger when reading the last check character; hold phase bit and digit ring timing resets the read gate and ends check area. The fall of read gate sets block read data; the VFO free runs until check area ends.

Read data operation ends when the fall of hold phase causes the next BS to reset phase select A or B trigger. When both phase select triggers are reset, the gate VFO trigger is reset. Figure 26 (Lines 5, 6, and 7) shows the read data end sequence. Figure 26 (Line 4) shows block read data remains on until 16 microseconds of the next AFC area have passed the read head; block read data suspends VFO operation until the noise gap has passed the read head. The read circuits continue the same operation sequence for each track area; the operation end is not shown because 1302 operations end with the same conditions as 1301 operations.

One exception to the previously described read operation occurs with HAO-CE read. The block read data signal is up for a 34 count (55 microseconds) at the start of each address and record area (Figure 26, Line 14). The count is different for HAO-CE read because the address and record area signals are forced on prior to the normal time. Figure 26 (Lines 11, 12, and 13) shows the HAO-CE format recognition sequence.

Data Separation

- **Separates data bits from clock bits.**
- **Clock gate latches for the duration of a clock bit.**
- **Data gate is blocked when clock gate is latched.**
- **Data gate latches for the duration of a data bit.**
- **Clock gate is blocked when data gate is latched.**

Data separation circuits separate clock data bits from the raw read data. The separation circuits begin operation when the gate VFO is set; the resultant ramp gate and data time signals are used to drive the separation circuits.

Two latches are used to separate data; these latches, the clock gate and data gate latches, are impulsed with the output of AND 1 (Figure 28). In the absence of raw read data, the on side of each latch produces an output that follows the input; however, the clock and data latches cannot latch in the absence of read data (Figure 28). Because the first raw data bit latches the clock gate, clock gate latches for the duration of the first raw data bit. The first bit separated is a clock bit (Figure 29, Line 9). The example operation on Figure 29 shows the timing circuit sequence when clock bits are on the raw data line.

The first data bit to be separated is shown in black (Figure 29, Line 7). The leading edge of this bit occurs at the center of the AND 1 output; the data gate latches and the first separated data bit is available for transfer to data triggers A and B. The second data bit to be separated is late; the bit is shown in black (Figure 29, Line 7). The leading edge of this late data bit is shown to precede the fall of the AND 1 (Figure 29, Line 6) output by a few nanoseconds. The presence of the data bit holds the data gate latch set for the entire duration of the data bit; this also prevents the clock gate latch from setting until the data bit expires. The dotted lines below the data bit show when the clock gate data latches would change state in the absence of the data bit (Figure 29, Lines 8 and 10). The effect of one latch on the other prevents bit splitting.

An early data bit with slanted lines drawn through it shows the circuit sequence that occurs if a data bit arrives too early. If an early data bit arrives before the data gate, it will be processed as a late clock bit; therefore, the earliest that a data bit can start is at the leading edge of the data gate (Figure 29, Lines 8 and 9).

A late clock bit is shown in black (Figure 29, Line 7). Similar to the late data bit, the clock gate and data gate latch transitions are delayed for the duration of the clock bit.

The advantages of this separation circuit are:

1. The ramp gate is adjusted to determine the limits of the leading edges of clock and data bits.
2. The leading edge of a late data bit need only precede the trailing edge of the ramp gate by a few nanoseconds to produce a full width, separated data pulse.
3. If a late clock bit is present when the leading edge of the ramp gate occurs, the data gate cannot be set until the clock pulse expires.
4. The separation ability of this circuit does not rely on maintaining an accurate pulse width. If there is adequate down time between pulses to reset a latch, and if the leading edges of the pulses are within the limits determined by the ramp gate, the data will be separated correctly.

Format Write Check

- **The VFO is reset at the end of each long gap.**
- **System write data is reduced to ½F data for comparison with ½F read data.**

The 1302 format write check sequence is identical to 1301 format write check operation except for the addition of a few VFO controls. Timing needed to check the first long gap after late index is supplied by the free running VFO. Set hold phase on index sets the gate VFO trigger at early index (Figure 30, Line 13).

The hold phase trigger output permits BS to set the phase select A or B trigger; the resultant timing is used to write check the long gap zeros that follow late index. Figure 30 (Line 15) shows where the VFO free runs. Because the VFO may have drifted slightly off frequency by the end of long gap, the VFO is clamped off when the gate VFO trigger resets (Figure 30, Line 13). (The gate VFO trigger is reset for one bit time at the end of each long gap except the first one that is made 3.2 microseconds longer by the write delay after late index.) The VFO is reset to compensate for frequency drift while free running in the long gaps (Figure 16, Area 1C).

During the time the VFO is clamped off, it returns to its nominal operating frequency of 2.5 megacycles. Write check data is not skipped when the VFO is off because each long gap is extended an extra bit during format write. Immediately after each long gap the gate VFO trigger is set with the first check data bit; the format check data is also used to sync the VFO in a write ones area (Figure 16, Area 6A shows how format check data is gated).

Because the format read data is ½F data, the 1F system write data must be prepared to compare with the ½F read data; the circuits used to write ½F format data are also used to reduce the 1F system write data to ½F compare data (Figure 16, Areas 9C and 10C).

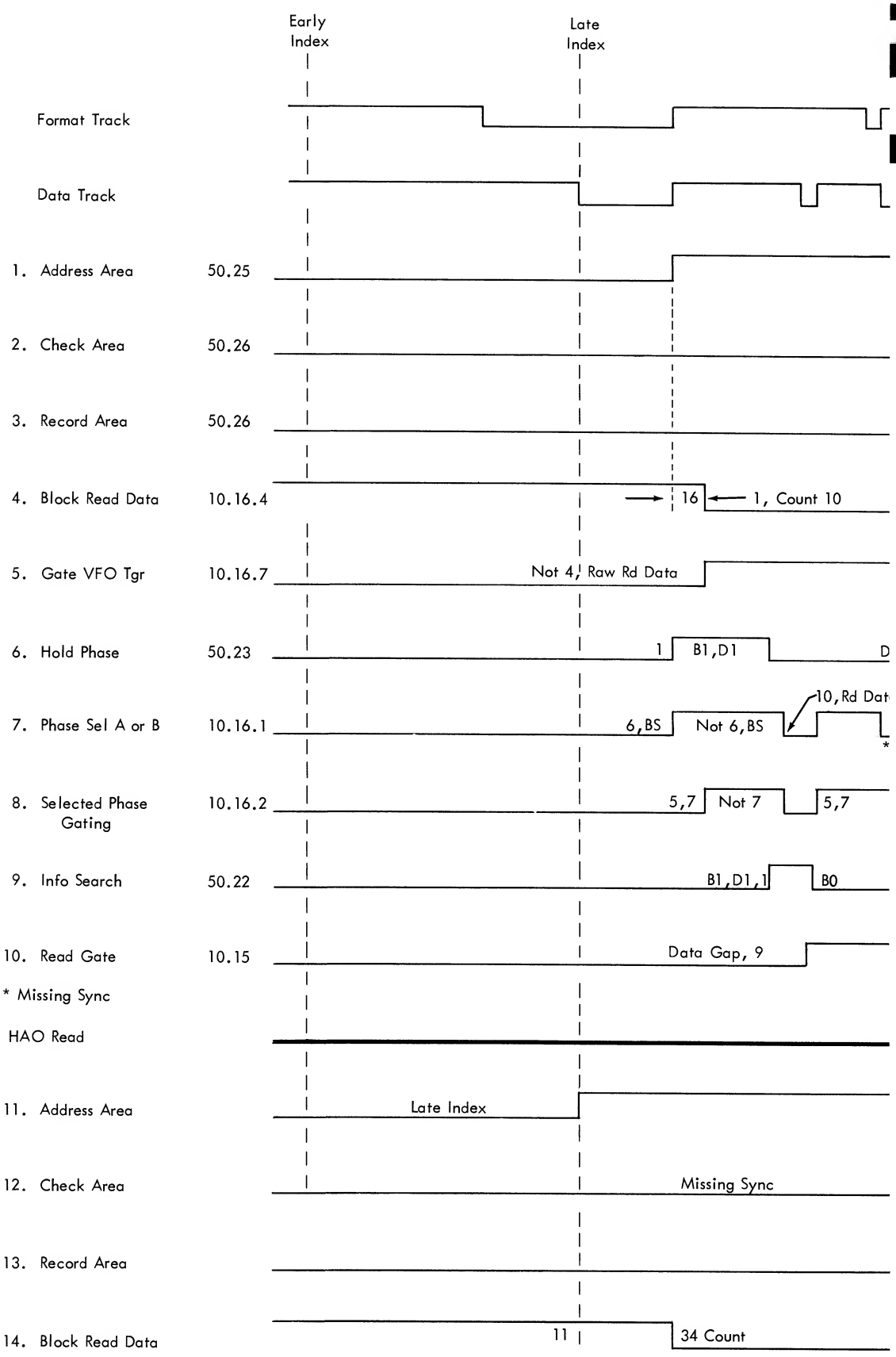
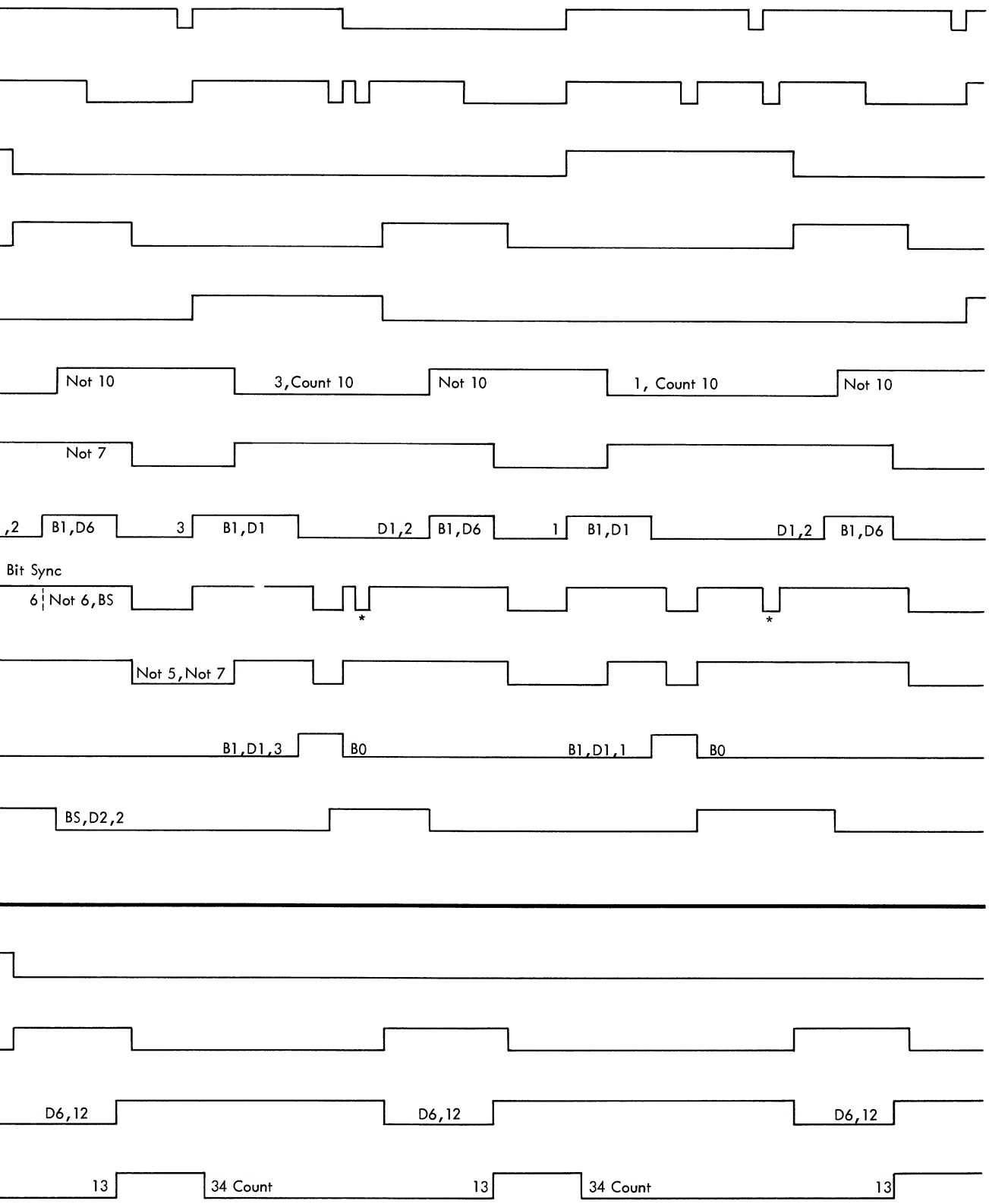
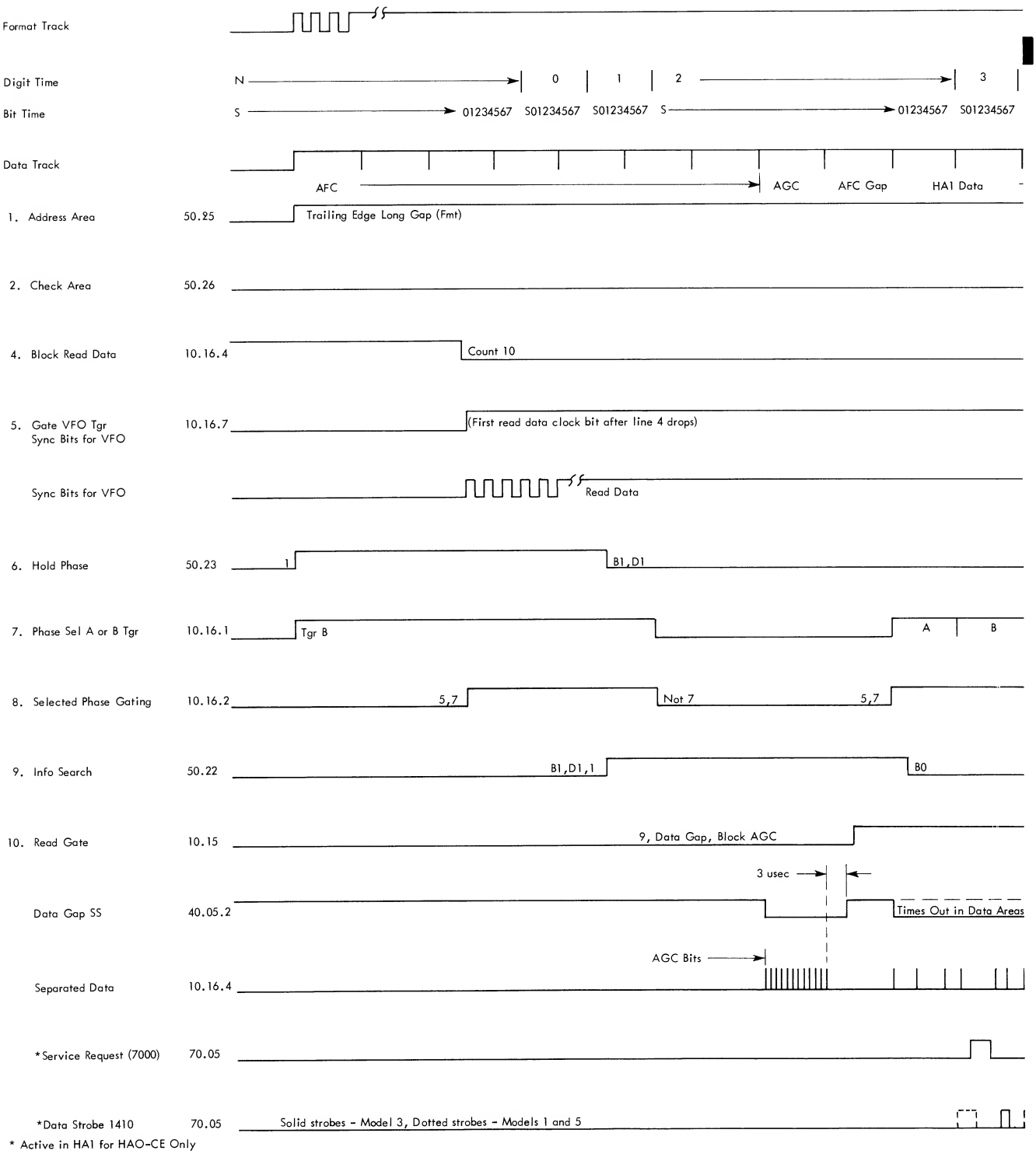


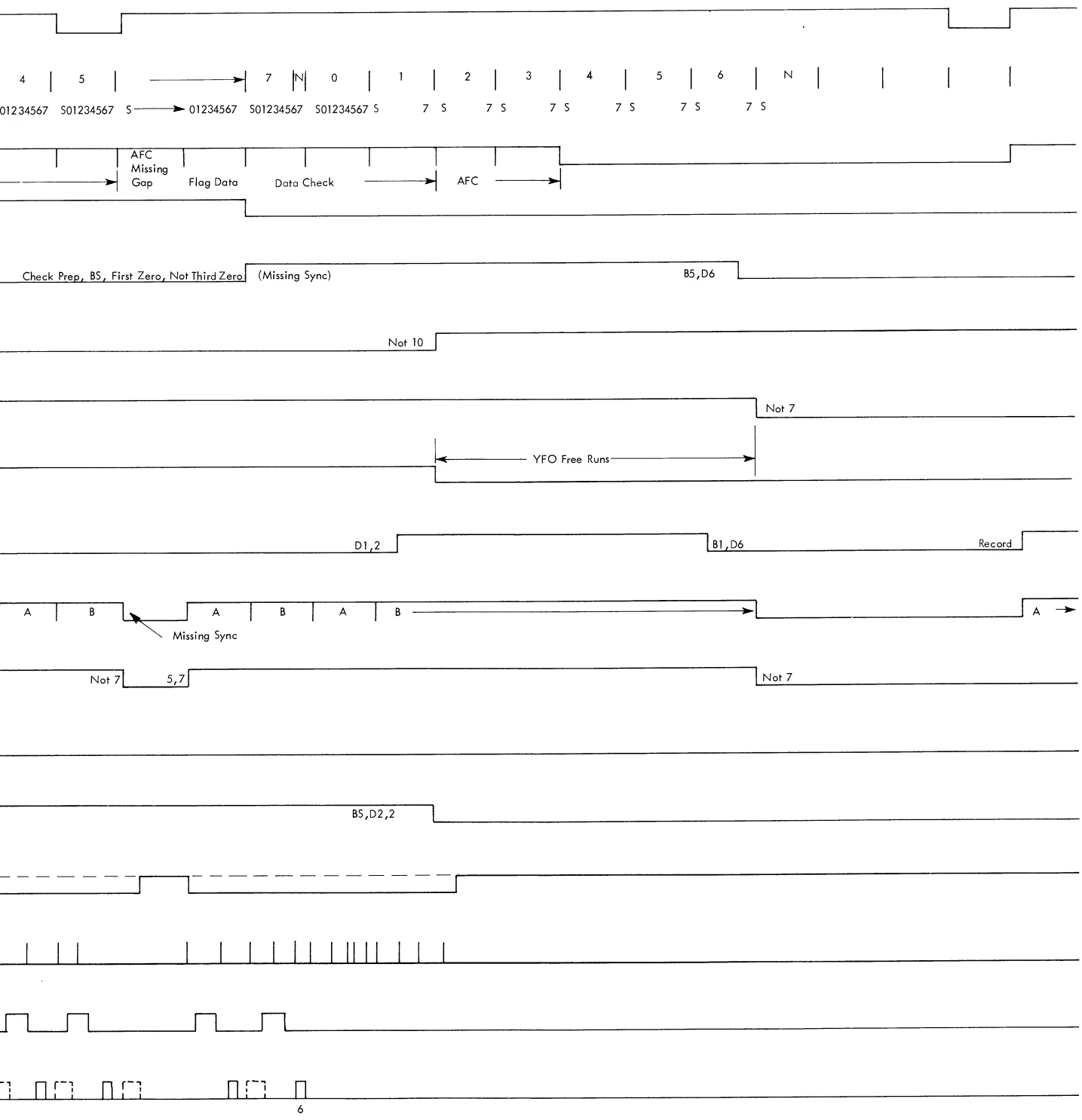
Figure 26. Read Data Timing


Not 10
3,Count 10
Not 10
1, Count 10
Not 10
Not 7
,2
B1,D6
3
B1,D1
D1,2
B1,D6
1
B1,D1
D1,2
B1,D6
Bit Sync
6
Not 6,BS
*
*
Not 5,Not 7
B1,D1,3
B0
B1,D1,1
B0
BS,D2,2
D6,12
D6,12
D6,12
13
34 Count
13
34 Count
13



* Active in HA1 for HAO-CE Only

Figure 27. Read Data Timing—HA1


4
5
7
N
0
1
2
3
4
5
6
N
01234567 S01234567 S
01234567 S01234567 S01234567 S
7 S
7 S
7 S
7 S
7 S
7 S
AFC Missing Gap
Flag Data
Data Check
AFC
Check Prep, BS, First Zero, Not Third Zero
(Missing Sync)
B5,D6
Not 10
Not 7
YFO Free Runs
D1,2
B1,D6
Record
A
B
A
B
A
B
A
Missing Sync
Not 7
5,7
Not 7
BS,D2,2

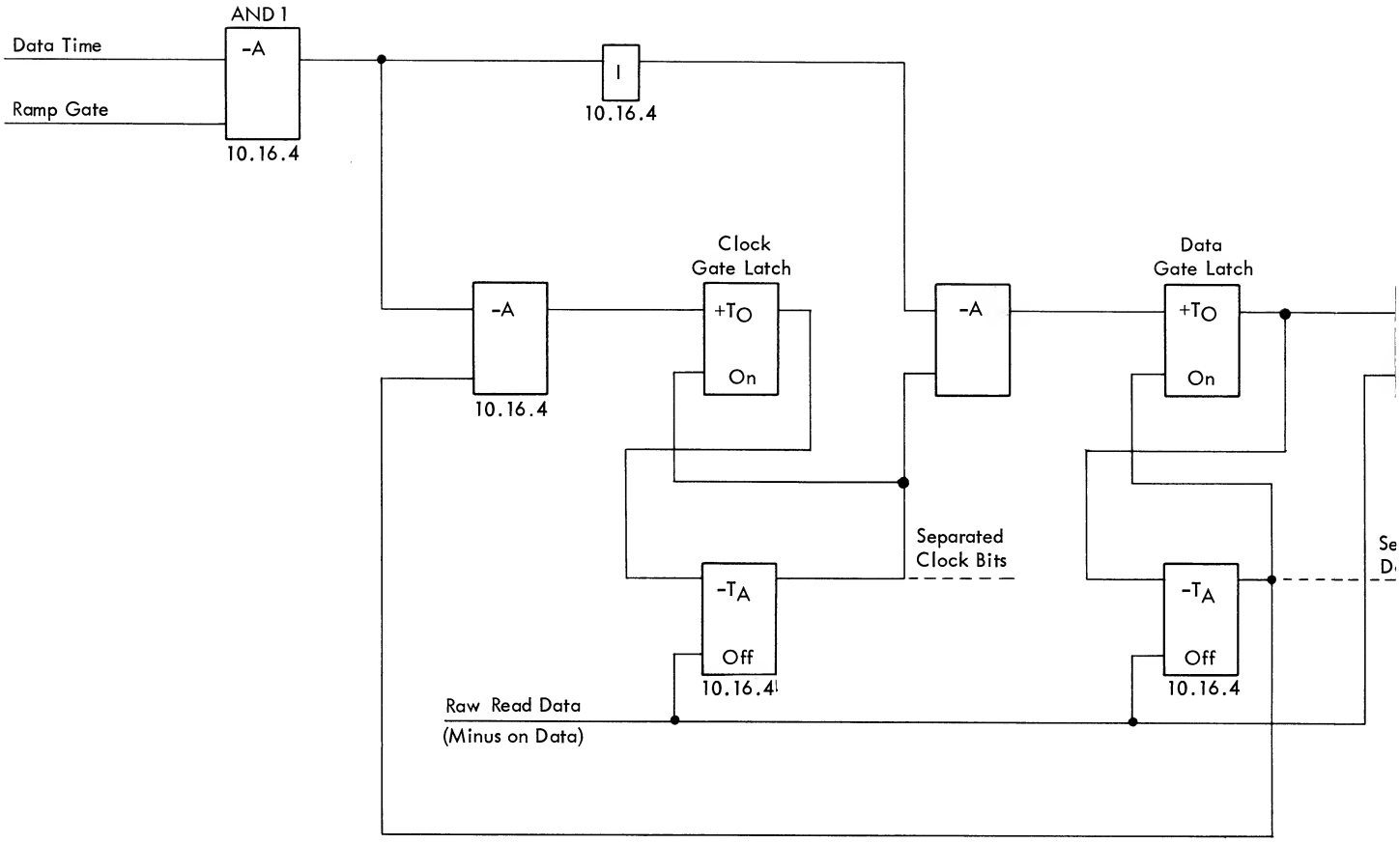
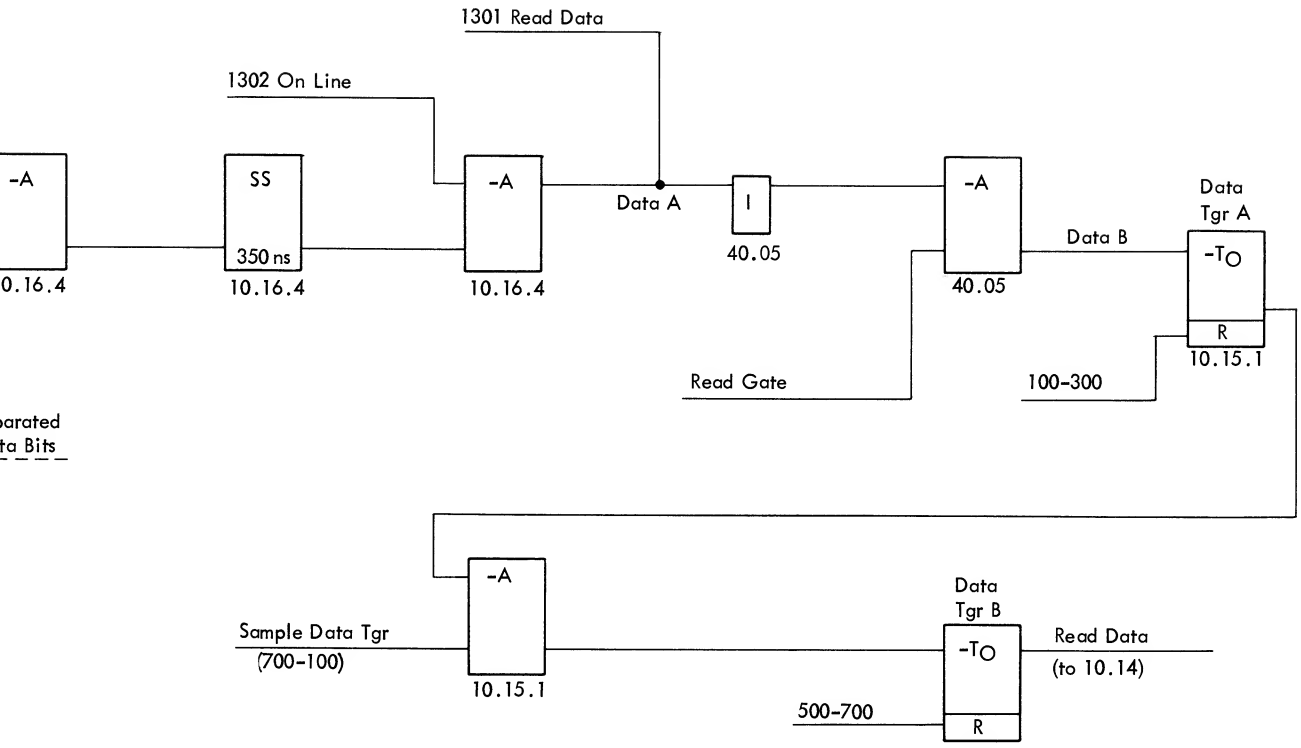


Figure 28. Data Separation Circuit


1301 Read Data
1302 On Line
-A
0.16.4
SS
350 ns
10.16.4
-A
10.16.4
Data A
1
40.05
-A
40.05
Data B
Data
Tgr A
-TO
R
10.15.1
Read Gate
100-300
parated
ta Bits
-A
Sample Data Tgr
(700-100)
10.15.1
Data
Tgr B
-TO
R
Read Data
(to 10.14)
500-700

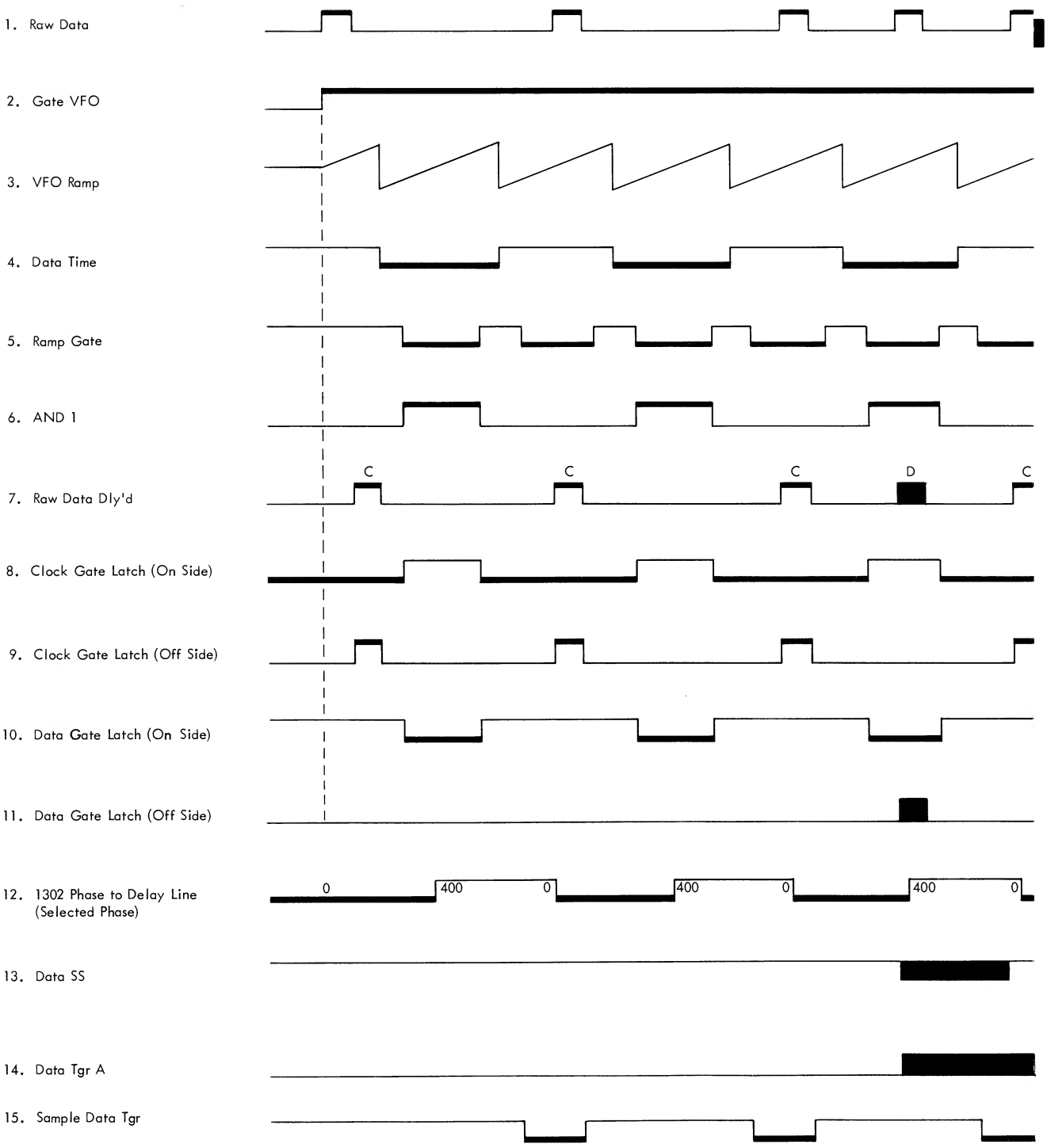
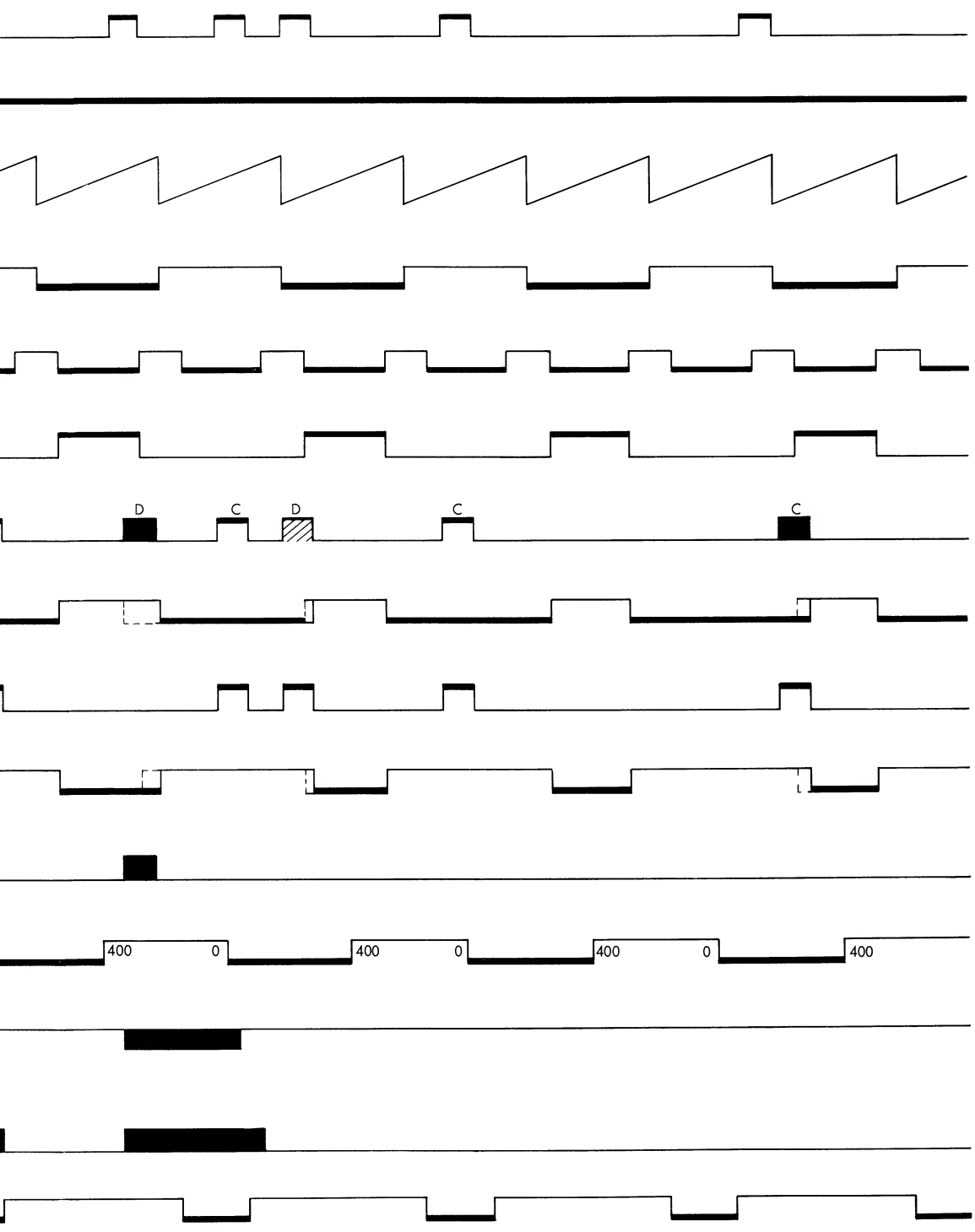
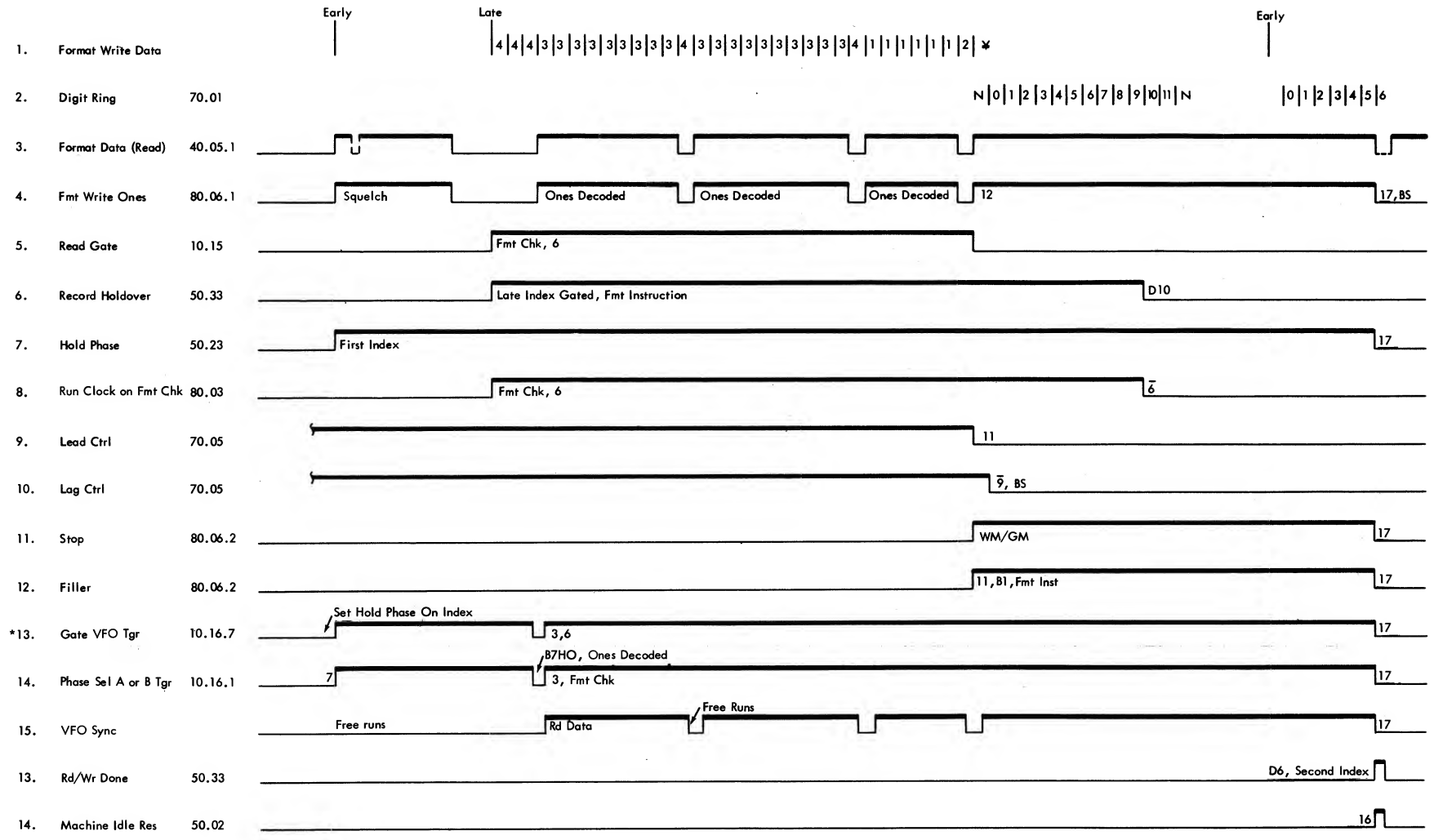


Figure 29. Data Separation Timing


D
C
D
C
C
400
0
400
0
400
0
400



* Gate VFO is reset for one bit time at the end of each long gap.

Figure 30. Format Write Check Sequence

CE Track Addressing

- **One CE cylinder per access.**
- **CE cylinder 250 is located when the system addresses cylinder 252, 253, or 254.**

Because the 1302 has only one CE cylinder per access, the 7631 track register is modified for 1302 operation; the track register modification maintains 1301 program compatibility.

When CE cylinders 252, 253, or 254 are addressed by the system with 1302 on line, cylinder 250 is located. Figure 31 (Note 1) shows T1B3, T2B0, and T2B1 encoder outputs are suppressed when T1 contains a pound (#) sign; therefore, all CE track addresses (9#00 to 9#99) address CE cylinder 250.

When a diagnostic is used to write HA1 on cylinder 250, the track addresses written are 9#20 through 9#59. Although 9#00 through 9#19 and 9#60 through 9#99 address cylinder 250 if any order other than HAO-CE is used, a no record found error occurs (Figure 31).

ADDRESS	1302 CYLINDER	1302 HEAD SELECTED
9#00 through 9#19	250	20 through 39
*9#20 through 9#59	250	00 through 39
9#60 through 9#99	250	00 through 39

*1302 diagnostics use these addresses for HA1.

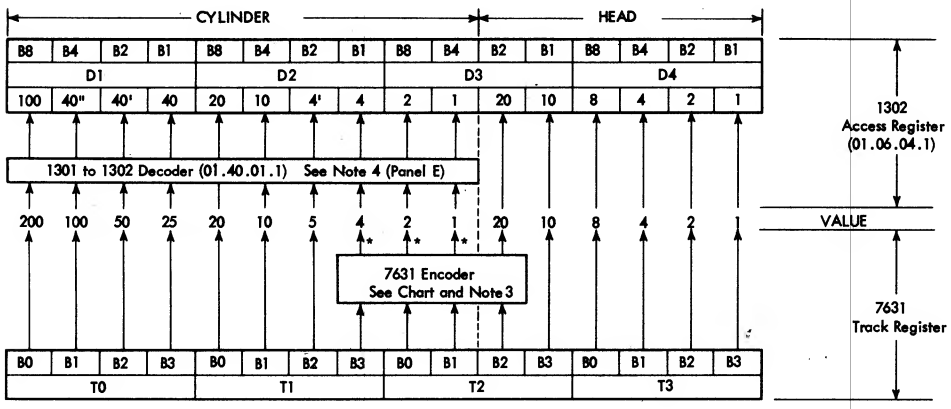
End Operations

Format and HAO operations end at D6 of second index when write and erase gates are reset simultaneously. The simultaneous erase and write gate resets create a 20 to 38 microsecond unerased area. The unerased format and data track areas are shown on Figure 8.

At the end of 1302 write operations other than format or HAO, the read write done trigger is set with the same conditions that are required for 1301 operations. However, the end triggers are not set at the same time for 1302 operation because of the 38-microsecond erase gate reset delay.

The 1302 end sequence starts when the read write done trigger is set. The read write done trigger then resets the write gate; the write gate fall starts the timing controls counter. At count 24, 38 microseconds later, the erase gate is reset; together, the reset erase gate and read write done trigger sets the end trigger to complete the write operation. The 38-microsecond delay from set read write done until end provides time to erase all the data written.

For CYO operation, the 1301 set head address register on CYO signal (ALD 01.50.33.1) is blocked with the erase gate signal. A 1302 set head on CYO signal is generated after the erase gate is reset (ALD 01.10.16.6). The purpose of the 1302 set head on CYO is to leave no unerased areas on the data tracks and to prevent head switching when the erase gate is on.



INPUT → OUTPUT

T1 B3	T2 B0	T2 B1	T2 B2	T1 B3	T2 B0	T2 B1	T2 B2
x					x		x
x			x		x	x	
x		x			x	x	x
x		x	x	x			
x	x			x			x
x	x		x		x		x

* Note 1: Suppress output when T1 is a # (B0, B2, B3) (Allows CE addresses to go to Cyl 250)
Note 2: All 7631 track register positions eliminate zeros (B0+B2) except in T1 if # (B0, B2, + B3)
Note 3: If a bit is in T1 B3, encoded output is as shown on chart. (If no bit in T1 B3, encoder has no effect.)
Note 4: The 1302 Decoder will decode 7631 Track Register output and pick proper Access Register positions. The decoder is in 1302 Panel E.

Figure 31. 7631 Track and 1302 Address Register Relationship

Oscilloscope Techniques

Correct oscilloscope techniques must be used for accurate displays and proper oscilloscope synchronization. Because of the 1302's high frequency and low voltage level signals, the following oscilloscope techniques should be used for 1302 adjustments:

1. Ground all scope probes at the nearest pin J.
2. The oscilloscope pre-amp and main amplifier must have a maximum rise time of 10 nanoseconds.
3. Use a dual trace scope such as a Tektronix 535A or 545 with a CA pre-amp, or a Tektronix 555 with a simultaneous dual trace. If a Tektronix 555 is used, align both sweeps at 100 nanoseconds per division. To align both sweeps, display the same signal with both probes and adjust the horizontal positioning control until both sweeps coincide.
4. The oscilloscope must have a main sweep delay feature and a secondary sync that will respond to a 1.25-megacycle sync input.
5. A grounded direct probe must be used when external secondary sync is required for the adjustment.

Adjustments and Procedures

CAUTION

These adjustments apply to virgin files. If customer data is on the file, be sure that the write inhibit switch is on.

The first step in making adjustments is to perform a seek to 0x888800; use an even module number for x. This cylinder has a prerecorded format track.

The following adjustments must be made in the sequence in which they are shown.

VFO Gain Adjustment

The VFO gain adjustment sets the correction current generated by the error detector section of the VFO. (See "Functional Units" for VFO operation.) To adjust the VFO gain, connect a voltmeter between pins 7K13A and 7K13D and adjust the 200-ohm potentiometer at 7J13 for one volt ± 0V (ALD 10.16.2). Because this adjustment affects the VFO's frequency, the frequency adjustment must be made after the gain has been adjusted.

VFO Frequency Adjustment

The VFO gain adjustment must precede this adjustment. The frequency adjustment is made to set the free running VFO to four times the frequency of the 1302 clock track. Load an HAO-CE order. Use address 0x888888; for x, use an even module number. Address 0x888888 selects cylinder 222 and head 8. Turn on write inhibit switch, then loop the machine in a continuous write operation with bit switch 4 (BCD 8) on. Connect the primary scope sync to the positive shift of the 7631 first index at 1B13D (ALD 01.70.15.1). Display clock track phase one (ALD 01.40.19.1, pin 1H04A) on one sweep and the VFO selected phase (ALD 01.10.16.2, pin 7K12F) on the other sweep. Delay the sweep 400 microseconds to display some area prior to the end of the index area. Set the secondary sync controls for internal sync on the positive transition of the displayed pulse. If the correct area is displayed, there will be an absence of VFO sync input (pin 7J13E) pulses at this time.

Adjust the oscilloscope delayed sweep horizontal speed to display exactly five clock pulses; one clock pulse should appear on every other vertical line. Adjust the 1K potentiometer at 7J13 to display one VFO selected phase cycle (ALD 01.10.16.2, pin 7K12F) on exactly each of the ten vertical lines. (The VFO selected phase cycle represents two VFO oscillations.)

NOTE: Return the horizontal speed control to the calibrated position.

Format Gap Singleshot Adjustments

The format long and short gap singleshots must be adjusted for reliable format recognition circuit operation. The adjustment procedures for the format long and short gap singleshots are in the section "Gap Detector Adjustments (1302)." Adjust only format singleshots.

CAUTION

The following write procedure applies only to virgin files. If the files contain customer data, skip the write procedure and proceed with the separation circuit adjustments.

Write HAO-CE

Turn off the write inhibit switch and add a temporary jumper from 1A10D to 1A10J only on virgin files because customer data would be destroyed. Perform a write HAO-CE operation using bit switch 4 (BCD 8) without errors.

Separation Circuit Adjustments

The separation circuit adjustments are needed for optimum separation circuit operation. Load an HAO-CE order. Then loop the machine in a continuous read

operation. Before a successful read can be performed the following circuits must be adjusted.

Delay Line Adjustment

The data delay line at 7K11 (ALD 01.10.16.4) contains a fixed delay of 90 nanoseconds and three optional delays. The optional delays are 20 nanoseconds between pins B and C, 10 nanoseconds between pins D and E, and 5 nanoseconds between pins F and G:

Pin	A	B	C	D	E	F	G	P
Delay		20		10		5		

This delay line delays raw read data to permit proper gate generator adjustment.

CAUTION

Careless handling of jumpers may destroy cards.

Use wire jumpers on the back panel to connect the 20-nanosecond optional delay. Connect output pin A to pin B, and connect pin C to load resistor pin P. All necessary delays must be connected in series between output pin A and load resistor pin P. This is a starting point and may have to be readjusted after the gate generator adjustments.

Gate Generator Adjustments

Connect the primary scope sync on the positive shift of Index HO at 1C17B. Observe the unseparated read data at 7K10M with one sweep and the data gate at 7K10P with the other sweep. These are DIF logic levels and they should swing between 0 to +3 volts (ALD 01.10.16.4). Move the delayed sweep until the 2F HA1 AGC character is displayed. Set the horizontal speed of the delayed sweep at 100 nanoseconds per division and use an external sync probe connected to 7K12C or 7J12U (ALD 01.10.16.2) to double sync the delayed sweep.

Adjust the top potentiometer at 7J14 so that the trailing edge (negative transition) of the data gate proceeds the leading edge (negative transition) of the following clock bit by 250 nanoseconds (Figure 32). Move the probe from 7K10P to 7K09Q. Adjust the lower potentiometer at 7J14 so that the leading edge (positive transition) of the data gate precedes the leading edge of the following data bit by 140 nanoseconds.

The purpose of this adjustment is to center the leading edge of the data bit within the data gate. If the adjustment limits are too low or too high, add or subtract delay as described in the delay line adjustments and then repeat the gate generator adjustments.

Data Gap Singleshot Adjustment

The data gap singleshot must be adjusted to permit reliable reading. The data gap singleshot adjustment is shown in the section "Gap Detector Adjustments (1302)." After this adjustment is completed, read HAO should operate without error.

Turn off HAO-CE and perform read HAO without errors; this insures a successful address compare. Remove the jumper from 1A10D to 1A10J. Using the CPU, run virgin file programs to write format and home address one on all virgin files. Run diagnostics for the appropriate system without errors.

Gap Detector Adjustments (1302)

The three gap ss in the 7631 must be adjusted to the following settings for proper operation:

Format Short Gap SS	(01B7H20)	3.4±0 (ALD 01.40.05.2)
Format Long Gap SS	(01B7H21)	10.0±0 (ALD 01.40.05.2)
Data Gap SS	(01B7H22)	3.0±0 (ALD 01.40.05.2)

The gap ss must be adjusted dynamically with a 1302 file. This adjustment may be made off-line with the 7631 CE panel or on-line with the system in a loop in any one of the prepare to verify and read operations of HAO, TRO, SRO, or TWA. If only the format short and long gap ss are to be adjusted, a format write check loop may be used.

Description of Adjustments

To adjust the gap ss, use an oscilloscope that can display two signals simultaneously, and has a continuously variable delayed sync.

The setting of a gap ss is to be measured from the fall of the last pulse of a long train of pulses, at the input, (pin C), to the rise of the output (pin H) of the gap ss.

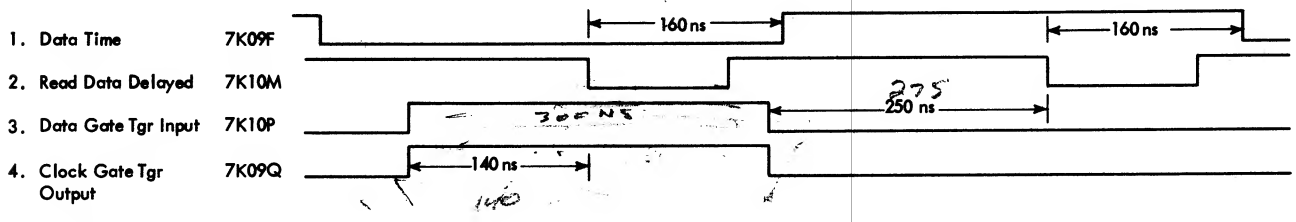
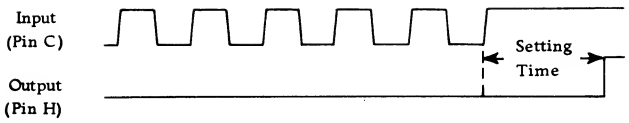


Figure 32. Ramp Gate Timing



NOTE: The data gap ss should not be adjusted on a few random data bits. An AGC burst must be used.

To adjust a gap ss off-line through the 7631 CE panel, set up any of the above-mentioned prepare to verify control instructions, then loop 7631 in a continuous read. This should form a repetitive loop on one operation that will supply format or data information to the inputs of the gap ss.

All of the above instructions assume that some format and data are present on the file. In the case of a new file or one that has been recently restacked, the format must first be written. With format write check loop, adjust the long and short gap ss; next, write HA1, and then loop on HA1 write check or read and adjust the data gap ss.

Shift Register Test (Eight-bit Mode); HAO-CE Write, AGC/AFC of HA-1. For convenience, set write inh

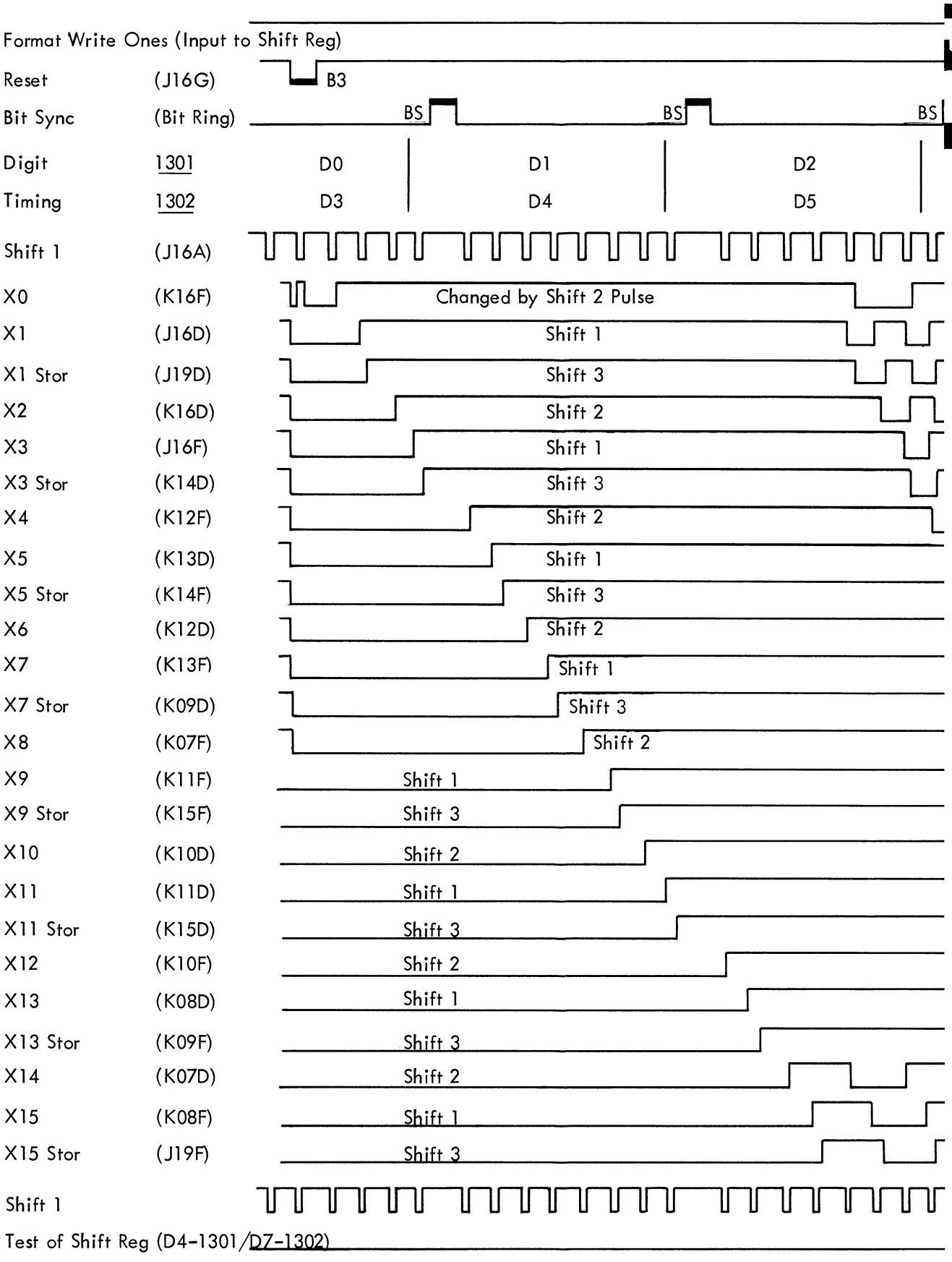
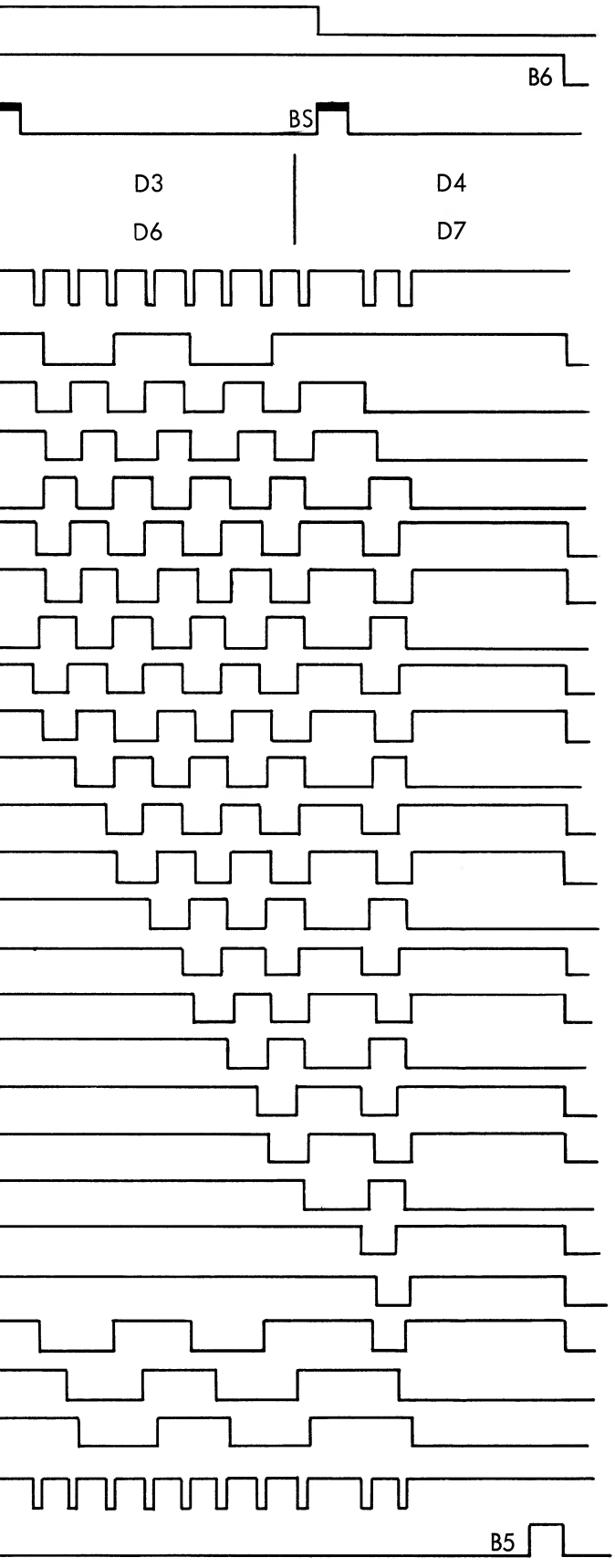


Figure 33. Shift Register Test in Eight-bit Mode

bit switch on. All locations Panel 1.



COMMENT SHEET

IBM 7631 FILE CONTROL ATTACHMENT FOR 1302 DISK STORAGE

FIELD ENGINEERING INSTRUCTION–MAINTENANCE, FORM 223–2813–0

FROM

NAME _____

OFFICE NO. _____

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CHECK ONE OF THE COMMENTS AND EXPLAIN IN THE SPACE PROVIDED

FOLD

☐ SUGGESTED ADDITION (PAGE , TIMING CHART, DRAWING, PROCEDURE, ETC.)

☐ SUGGESTED DELETION (PAGE)

☐ ERROR (PAGE)

EXPLANATION

CUT ALONG LINE

FOLD

FOLD

NO POSTAGE NECESSARY IF MAILED IN U.S.A.
FOLD ON TWO LINES, STAPLE, AND MAIL

STAPLE

STAPLE

FOLD

FOLD

FIRST CLASS
PERMIT NO. 81
POUGHKEEPSIE, N. Y.

BUSINESS REPLY MAIL
NO POSTAGE STAMP NECESSARY IF MAILED IN U. S. A.

POSTAGE WILL BE PAID BY
IBM CORPORATION
P.O. BOX 390
POUGHKEEPSIE, N.Y. 12602

ATTN: FE MANUALS, DEPARTMENT B96

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STAPLE

STAPLE